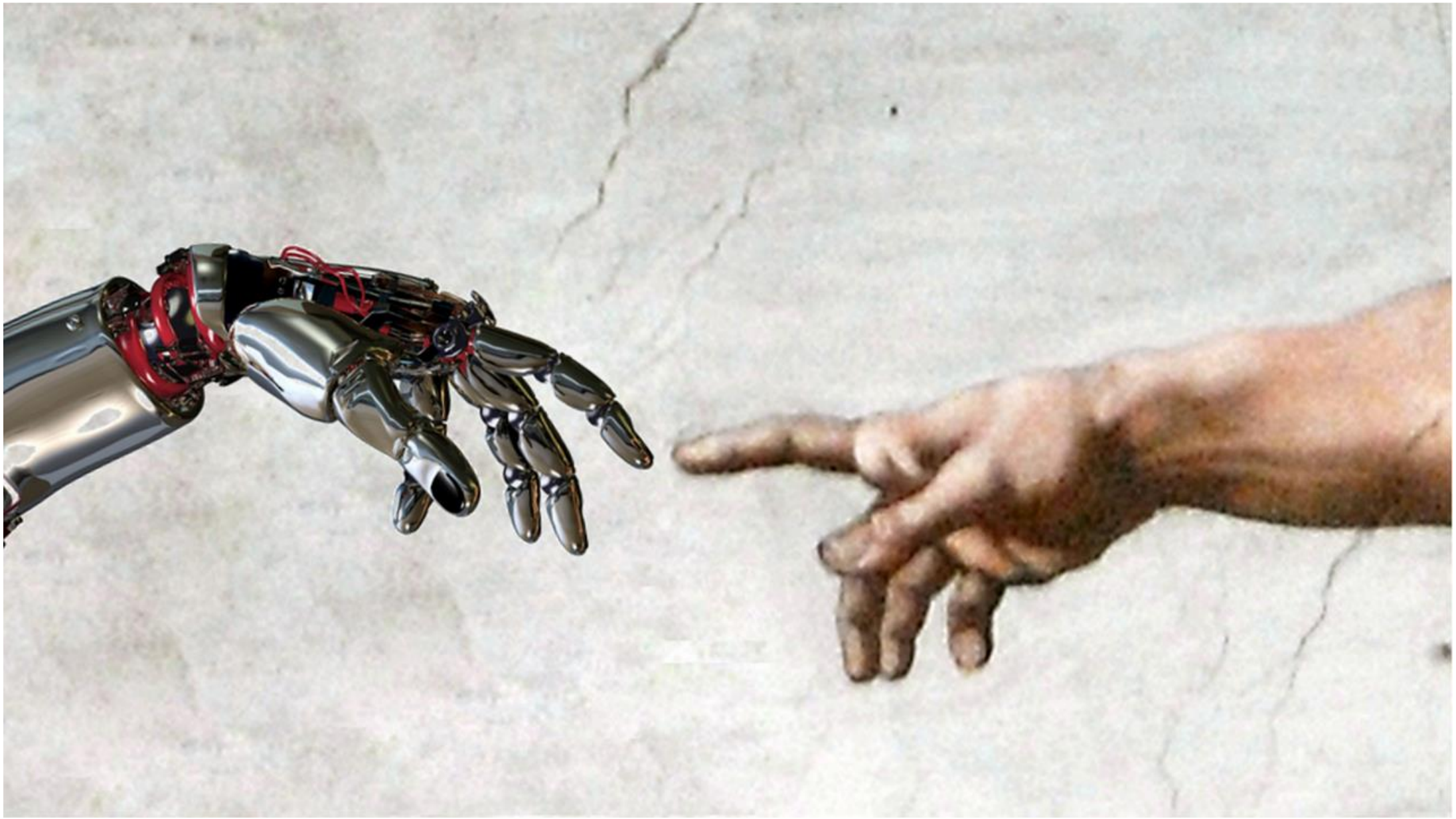
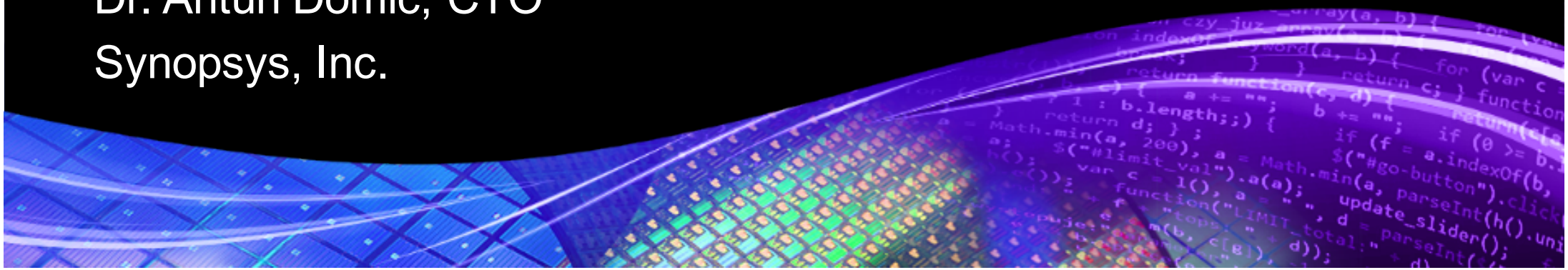


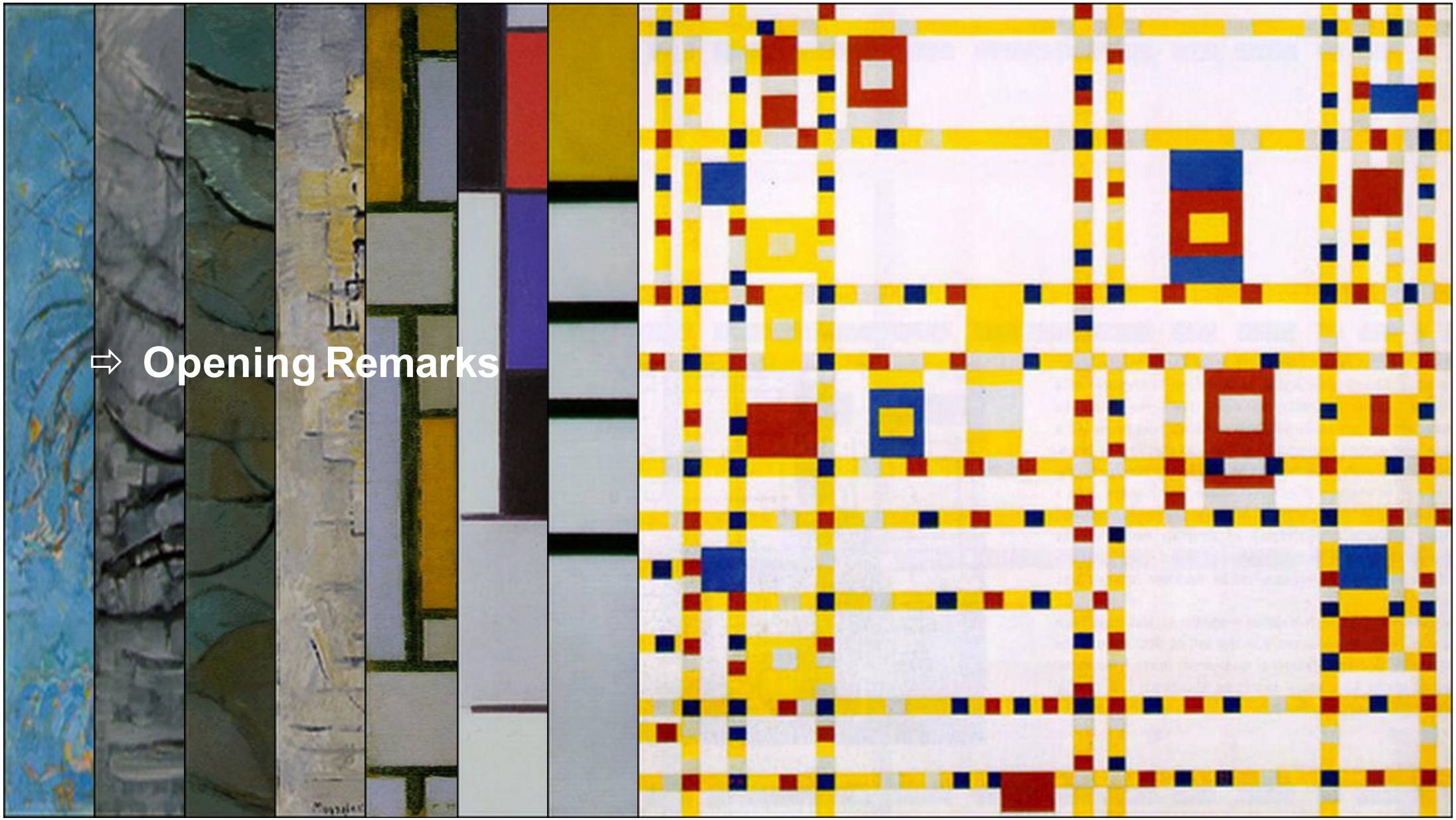
Some Implications On Logic Synthesis From The Coming Semiconductor Technologies

Dr. Antun Domic, CTO
Synopsys, Inc.



Agenda

⇨ **Opening Remarks**


⇨ Opening Remarks

Opening Remarks

L. Trevillyan, "An Overview of Logic Synthesis Systems", DAC 1987, Miami, FL

"Although synthesis is not primarily concerned with physical design, some consideration of physical design issues is needed when performing logic design.

Even if a synthesized implementation has met all of its logic-level constraints, it still is not a usable design unless it can be placed and wired, and, furthermore, it still satisfies the timing requirements after physical design has been performed."

Some Implications On Logic Synthesis

"In the Beginning…"

Intrinsic delay + load (#)

Interconnect RC was not a concern

Timing $\propto$ # of stages

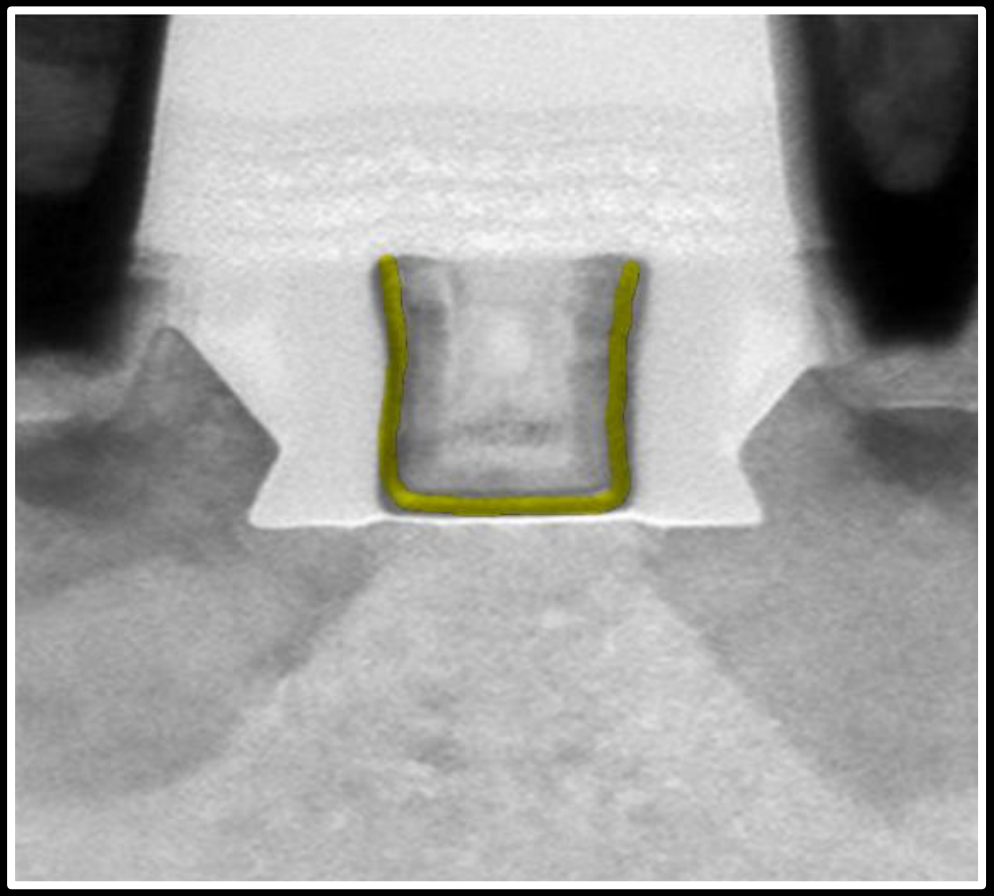
Standard cells libraries included a "delay" element to correct imbalances

Area was the real concern

Logic minimization was king

Some Implications On Logic Synthesis : Planar CMOS

W ⇔ Area vs. Timing, T_{OX} ⇔ Timing vs. Power (Leakage)



Over time,
standard cells libraries
have moved from
few hundreds to
a few thousand
elements

32 Nanometer NMOS high-k metal gate; Source: C.-H. Jan, et al, Intel, IEDM 2010

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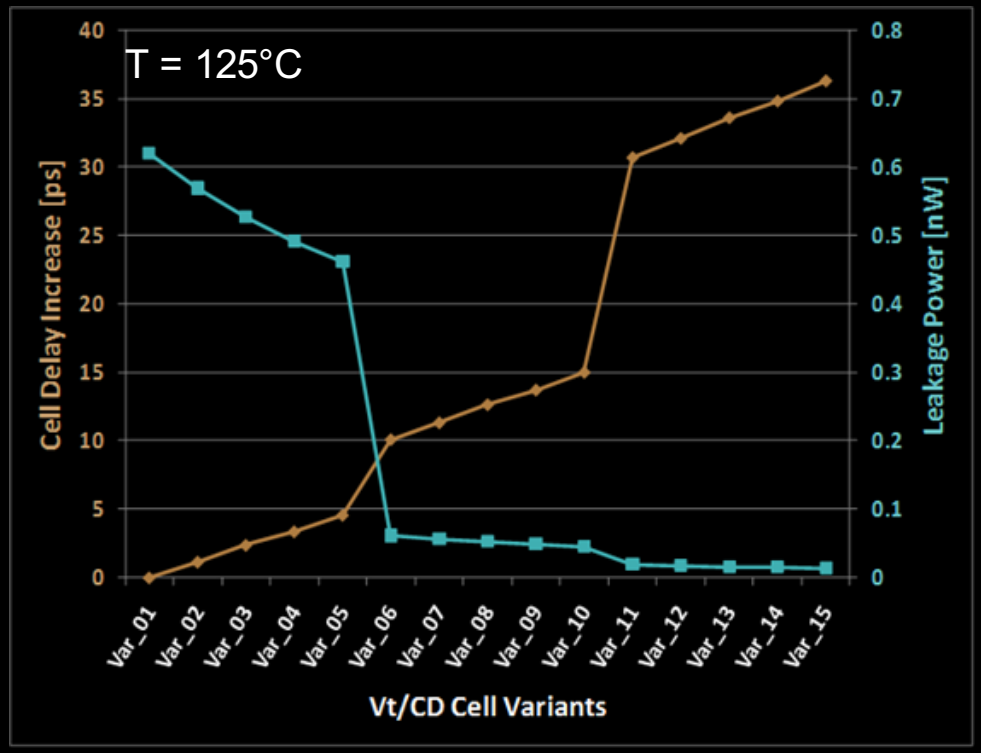
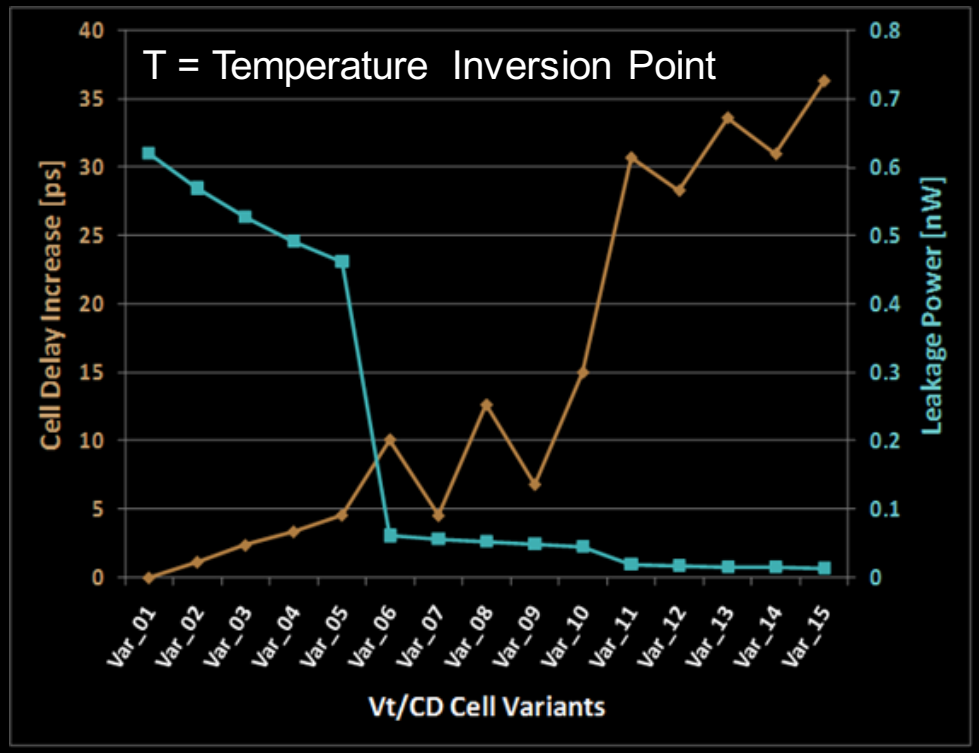
Some Implications On Logic Synthesis : Planar CMOS

Today Libraries Contain Thousand of Elements

Many Variants with the Same Footprint (Area) but Different Performance/Power





Source: Synopsys Research, 2016

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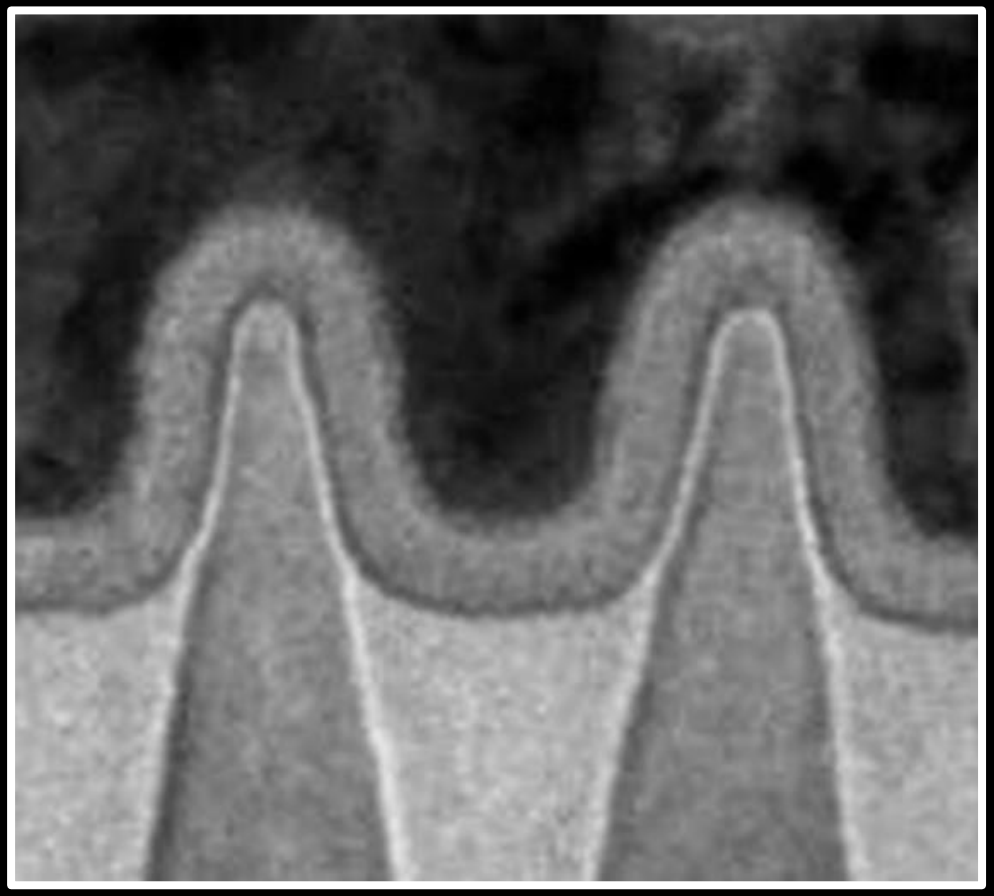
Some Implications On Logic Synthesis : FinFET

*Quantization of W to Begin with; Eventually 1-Fin; *Heat**



Standard cells are
"stripped naked"
Heavy burden on
physical synthesis
Utilization declines

22 Nanometer FinFET; Source: K. Mistry, Intel Technology & Manufacturing Day, 2017

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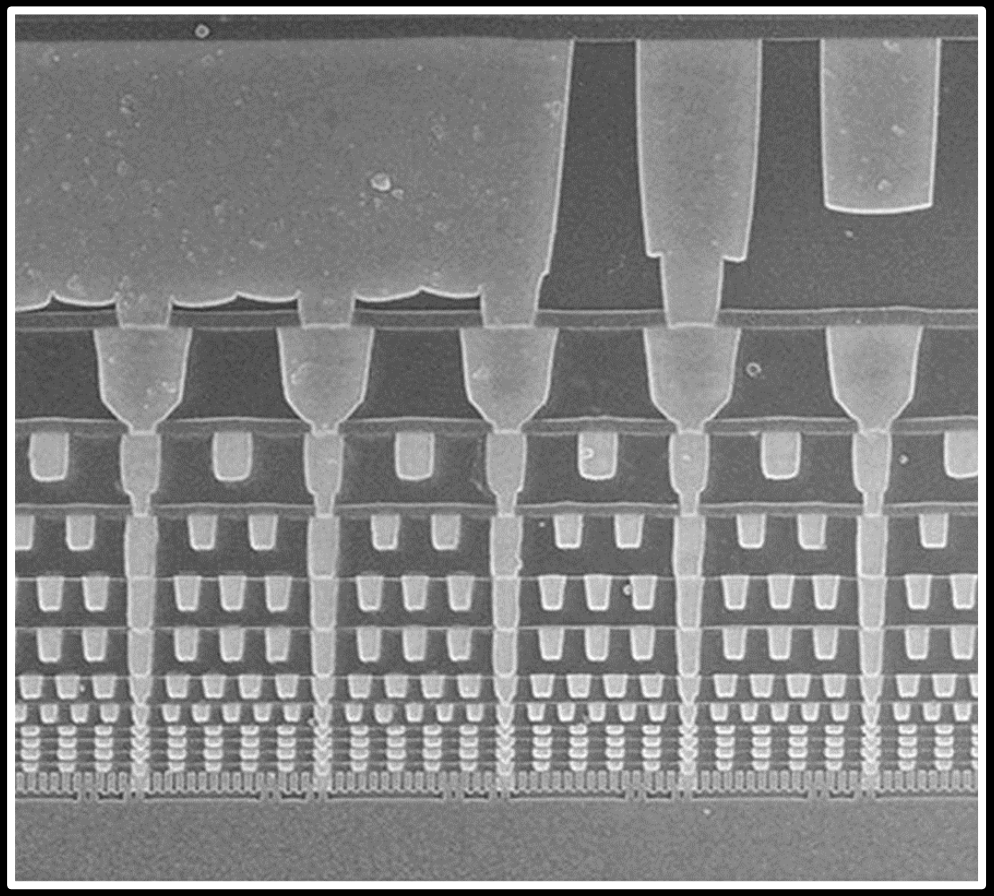
Some Implications On Logic Synthesis : Interconnect RC

Up to 3 Orders of Magnitude Variation Across the Stack

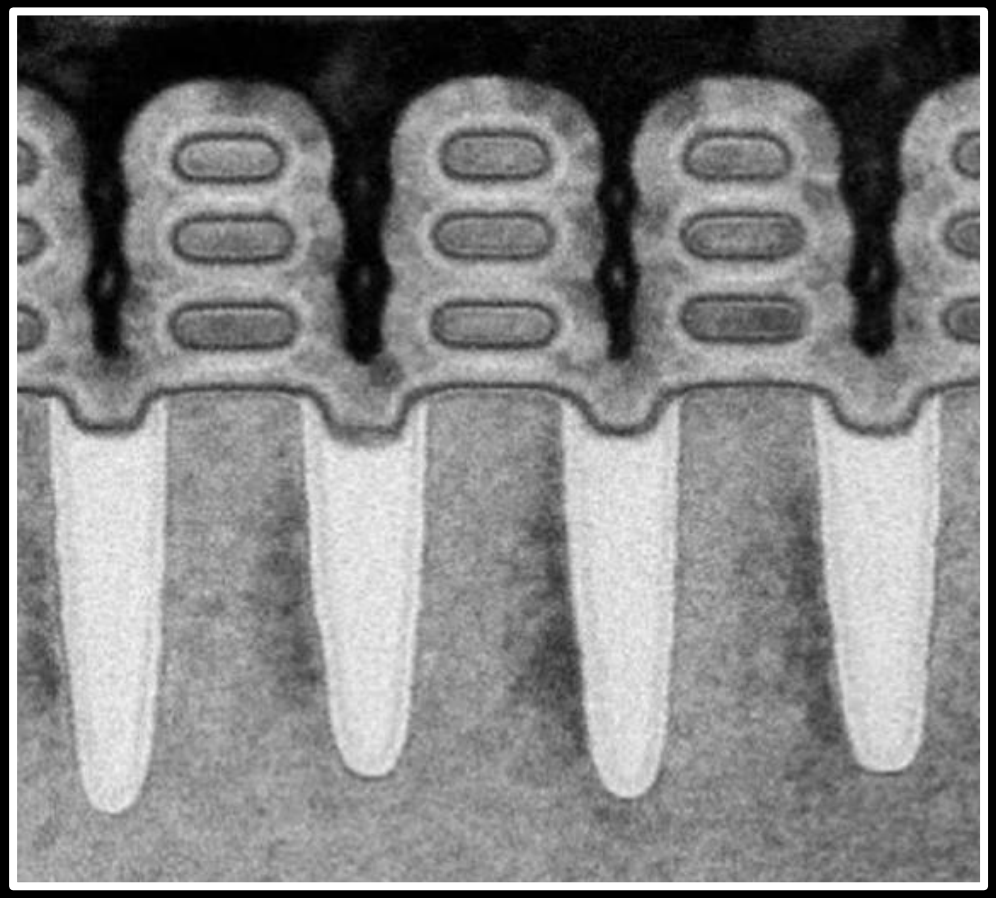


Resistance ratio
across the stack
goes above 1,000X
AND
different masks/patterns
for the same layer
show different R profiles

14 Nanometers; Source: Chipworks, 2014

Some Implications On Logic Synthesis : GAA

*Eventually 1-Nano-Wire/Sheet/Slab ? *Heat**



Theoretically,
one could stack a different number of devices to implement faster/stronger standard cells without impacting area, but…

5 Nanometer Stacked Nano-Sheets; Source: IBM, 2017

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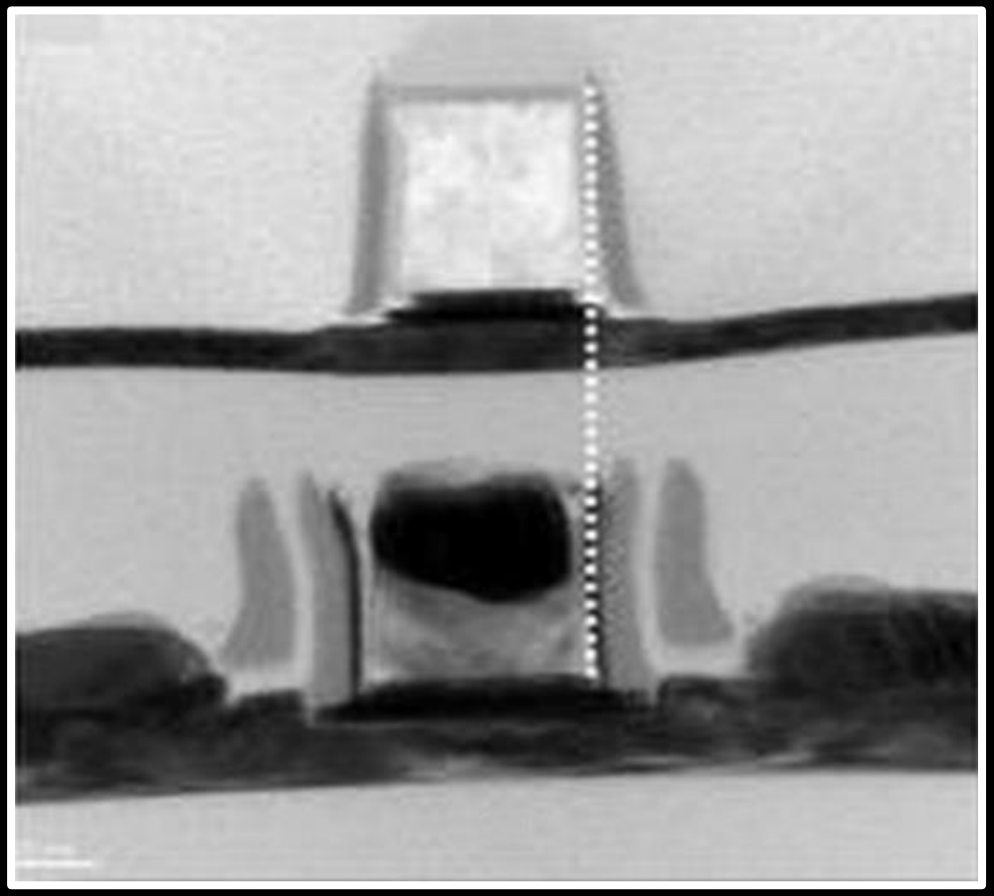
Some Implications On Logic Synthesis : Monolithic 3D

*Routing Only at the Top (BEOL); MEOL Under-Utilized; *Heat**



Each tier is made of
FEOL + MEOL
connected by inter-tier via
(same pitch as contact,
but highly resistive)
One BEOL at the top
There may be 2 × n tiers

Source: P. Batude, et al., LETI, VLSI 2011

Opening Remarks

Logic Synthesis doesn't live alone but is intrinsically tied to Physical Synthesis

Over the last 30 years, synthesis went progressively physical, chasing interconnect RC and power

Emerging lithography and devices are dramatically increasing the dependence of synthesis on placement, global routing, track assignment, and possibly even further into routing

Heat becomes a much earlier concern

Agenda

Opening Remarks

- **Where Do We Stand ? What Lies Ahead ?**
  - **EUV Lithography & Non-Planar Devices**

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Opening Remarks

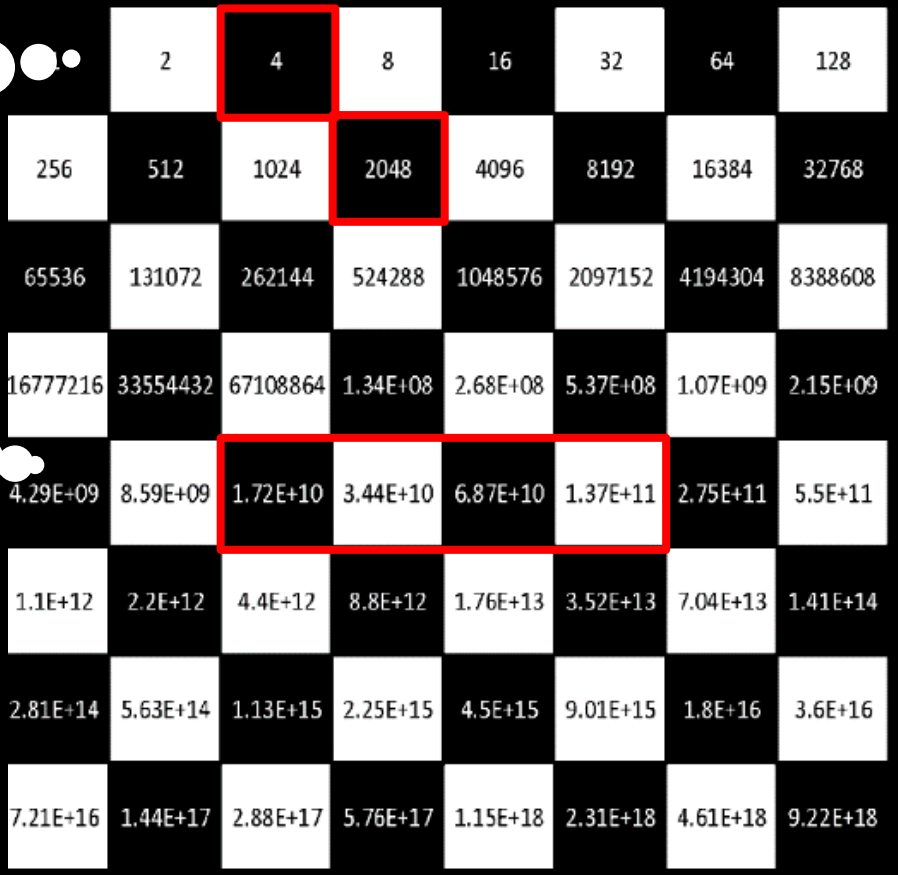
⇨ **Where Do We Stand ? What Lies Ahead ?**

⇨ **EUV Lithography & Non-Planar Devices**

The Rice-And-Chessboard Problem

The Lower Half of the Chessboard

1958
1st Integrated Circuit
4 Transistors



1971
1st CPU
2,300 Transistors
@ 10um

2017
State-of-the-Art CPU
19B Transistors
@14nm

2017
State-of-the-Art GPU
20B Transistors
@ 12nm

2017
State-of-the- Art FPGA
17B Transistors
@ 14nm

2012
State-of-the-Art
128Gb DRAM
137B Transistors
@ 30nm

Source: Ibn Khallikān, ca. 1256; M. van den Brink, ASML Investor Day, 2014

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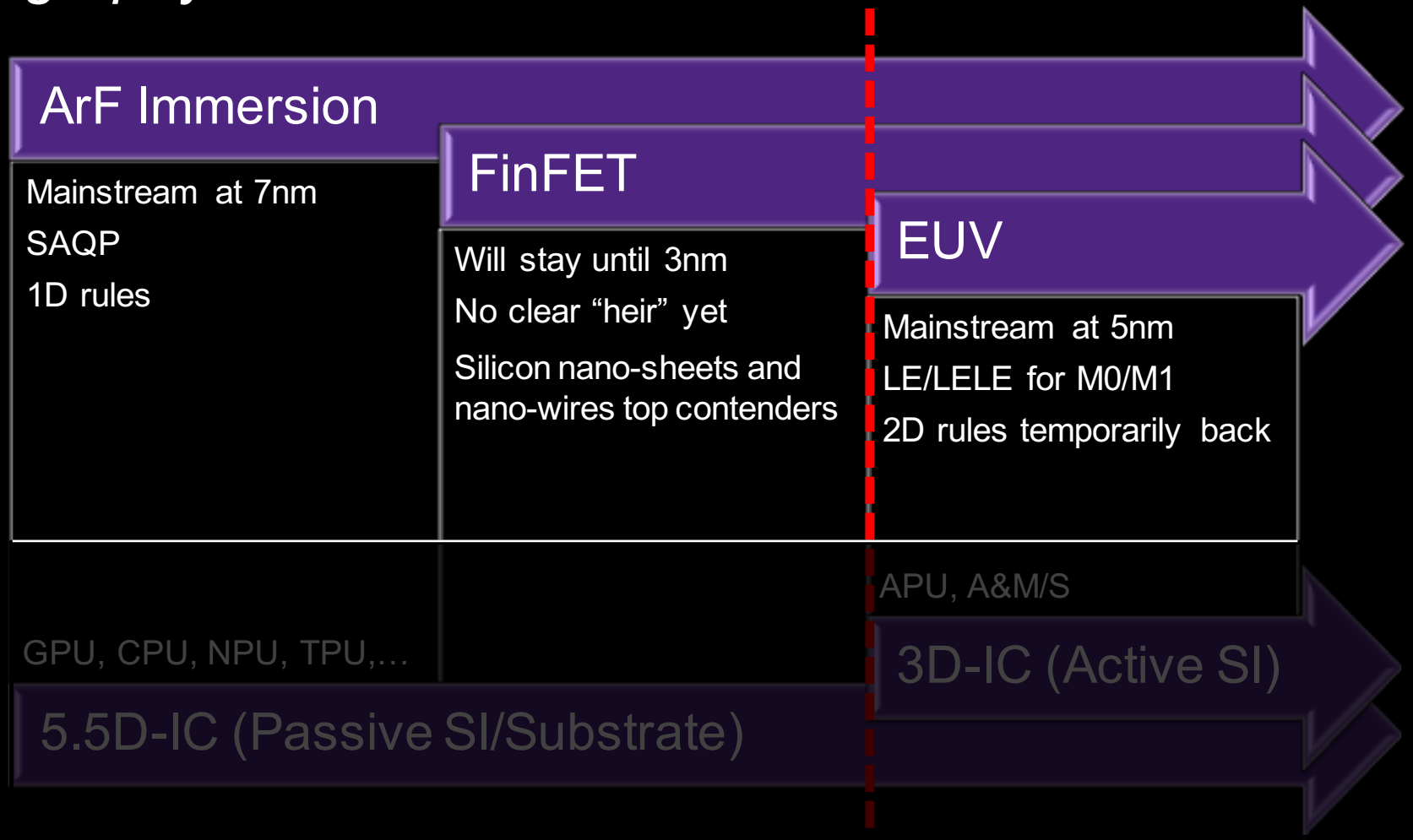
Where Do We Stand ? What Lies Ahead ?

Lithography & Devices



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Lithography Implications – ArFi, EUV, Applications

Different Objectives Lead to Very Different Outcomes !

	Minimum Metal Pitch	Minimum Contacted Pitch	MMP × MCP	MCP / MMP	Most Advanced Lithography
N10 (HP)	36nm	54nm	1,944nm^2	1.5X	**SAQP**
N7	40nm	57nm	2,280nm^2	1.425X	LELELE
N10 LPE	48nm	64nm	3,072nm^2	1.333X	LELELE
N7 LP	40nm	56nm	2,240nm^2	1.4X	LELELE
N7 LPE	36nm	54nm	1,944nm^2	1.5X	**EUV**

Source: Synopsys Research, 2017

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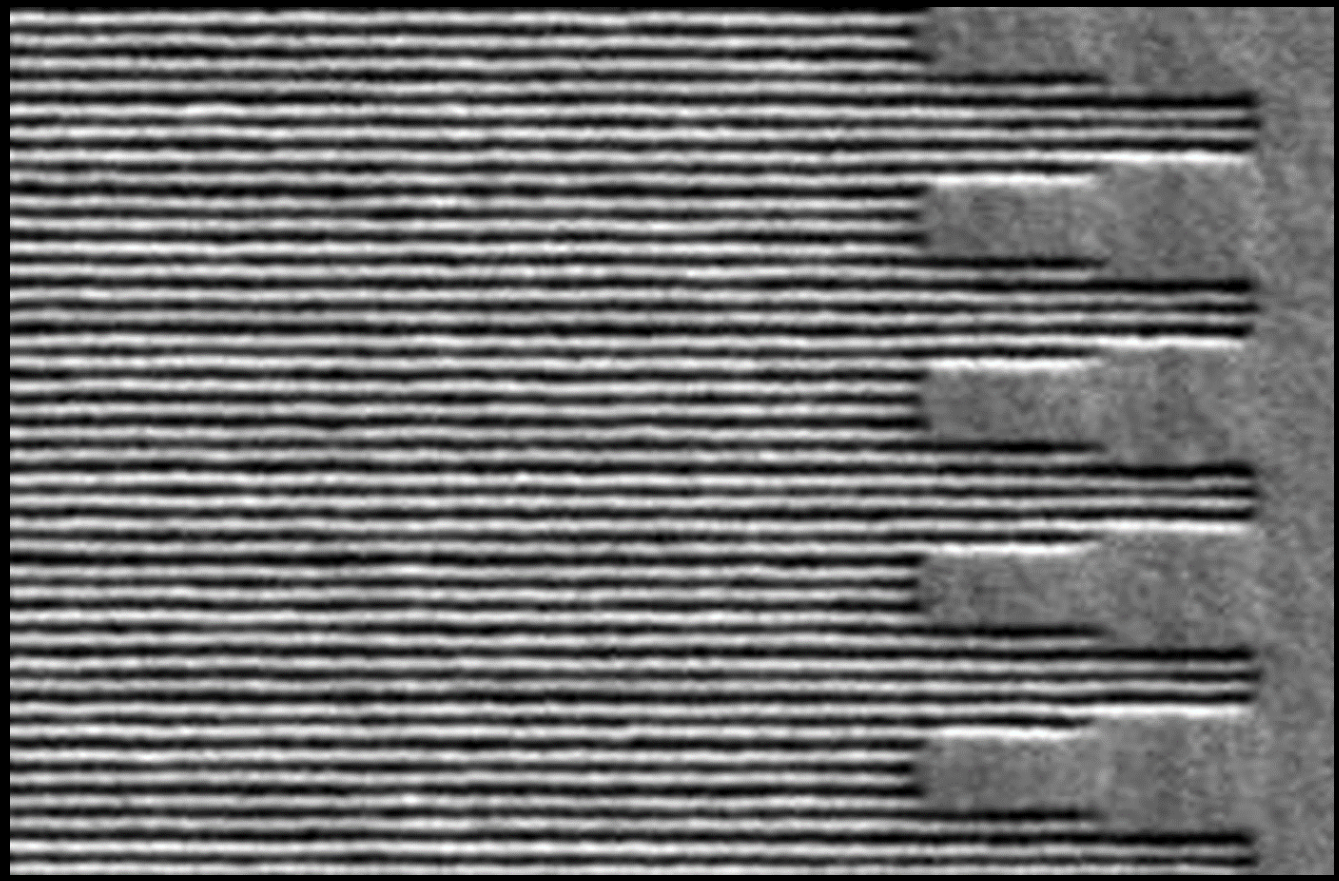
Lithography Implications – ArF Immersion, SAQP

From 2D To 1D Rules, No Jogs, Only One Pitch/Width



24 Nanometer Pitch, ArF Immersion, SAQP; Source: R. Brain et al., Intel, IEDM 2016

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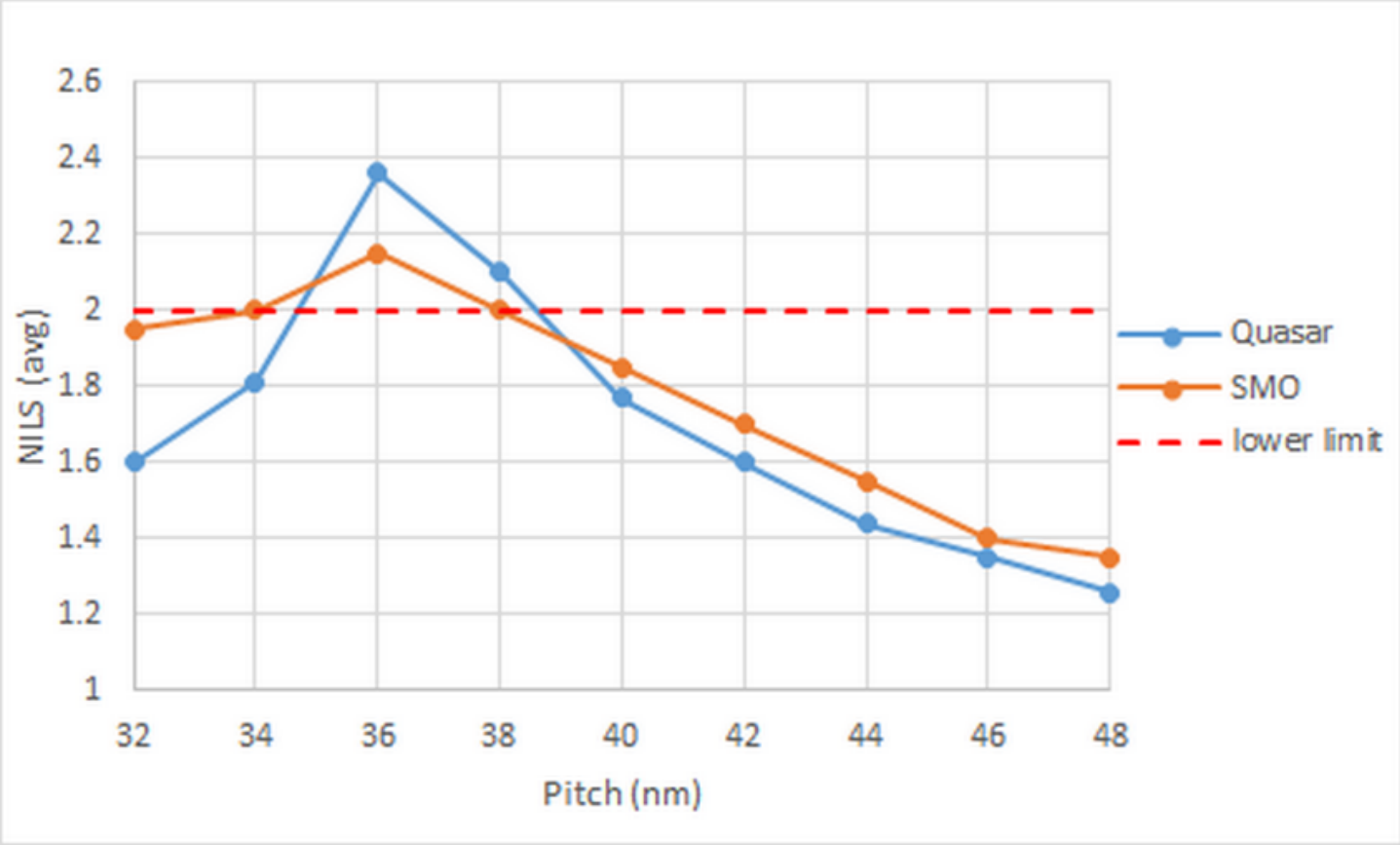
Lithography Implications – EUV SE Life Span

Defocus, Asymmetry, and Latitude Narrow the Breadth of Options

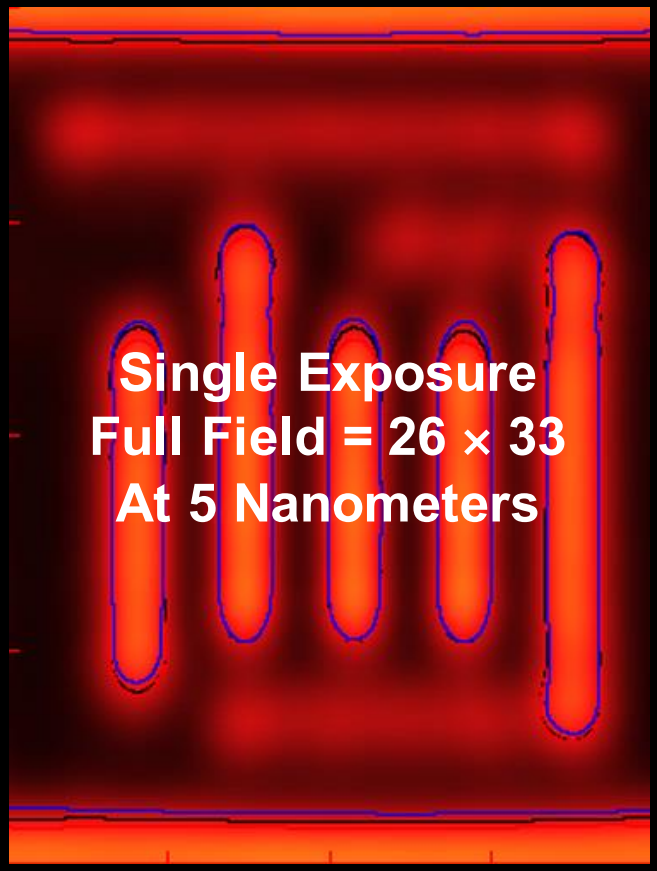
Higher NA Can Help, at the Price of Higher Magnification ⇨ Smaller Field

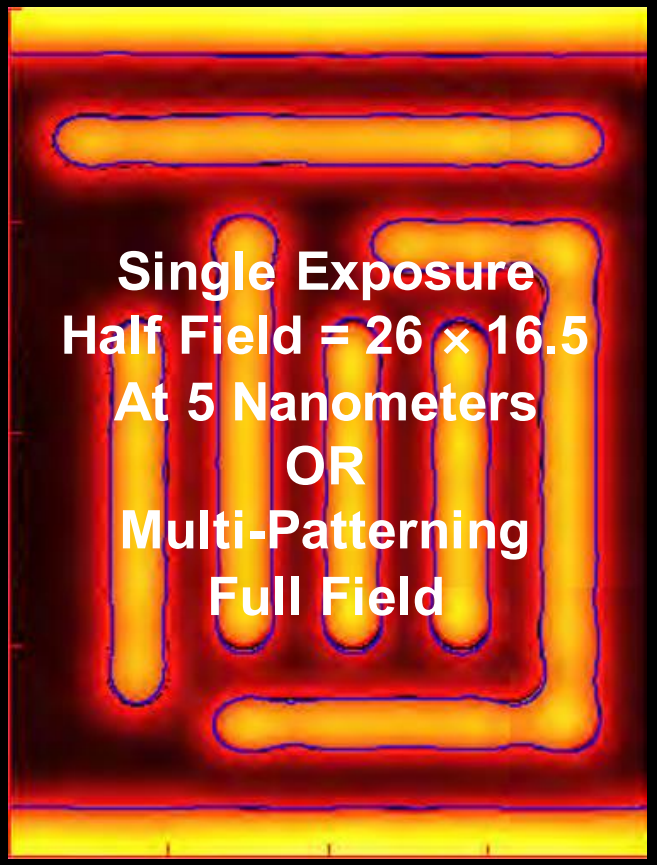


Source: RH Kim et al., IMEC, SPIE 2016

Lithography Implications – EUV SE Life Span

Return To 2D Rules May Be Temporary (at 7 Nanometers)





11 Nanometer M1 Lines @ 5 Nanometers, EUV SE FF vs. HF Image Intensity; J. van Shoot, et al., ASML, EUVL Workshop, Berkeley, CA, 2016

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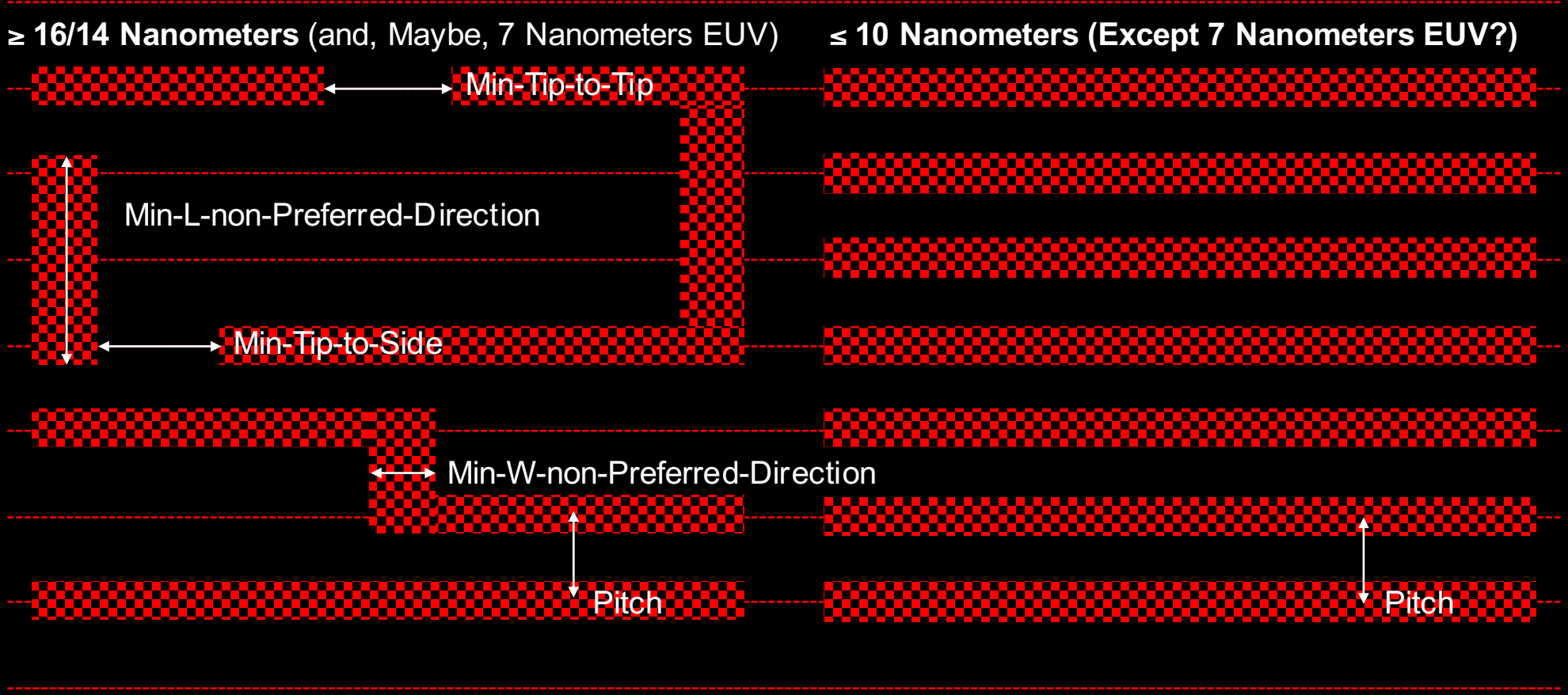
Design Implementation At ≤ 10 Nanometers

From 2D to 1D Routing AND Standard Cells

No More Jogs, Tip-to-Tip, and Tip-to-Side Rules, Only One Pitch/Width



Source: Synopsys Research, 2016

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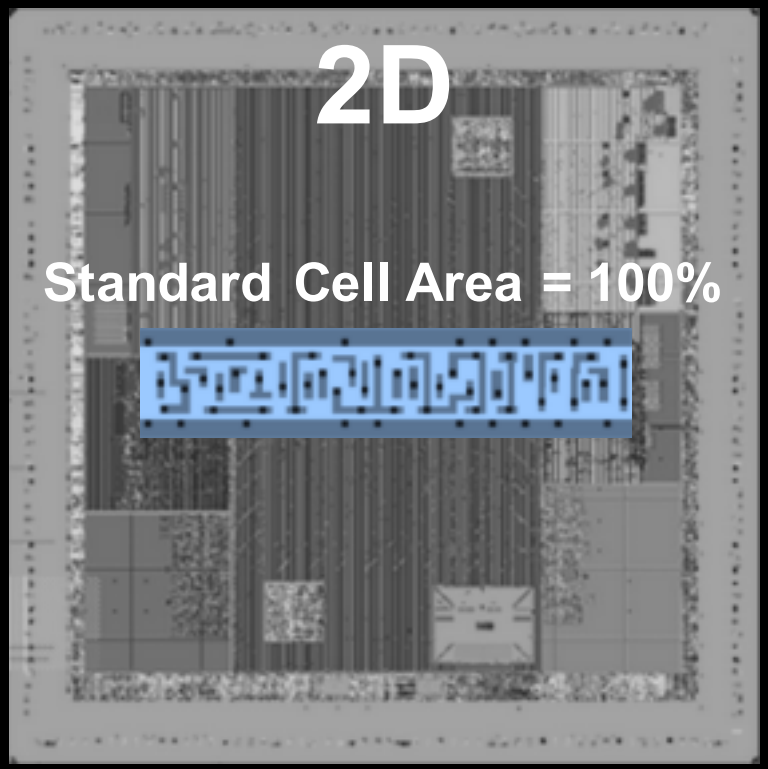
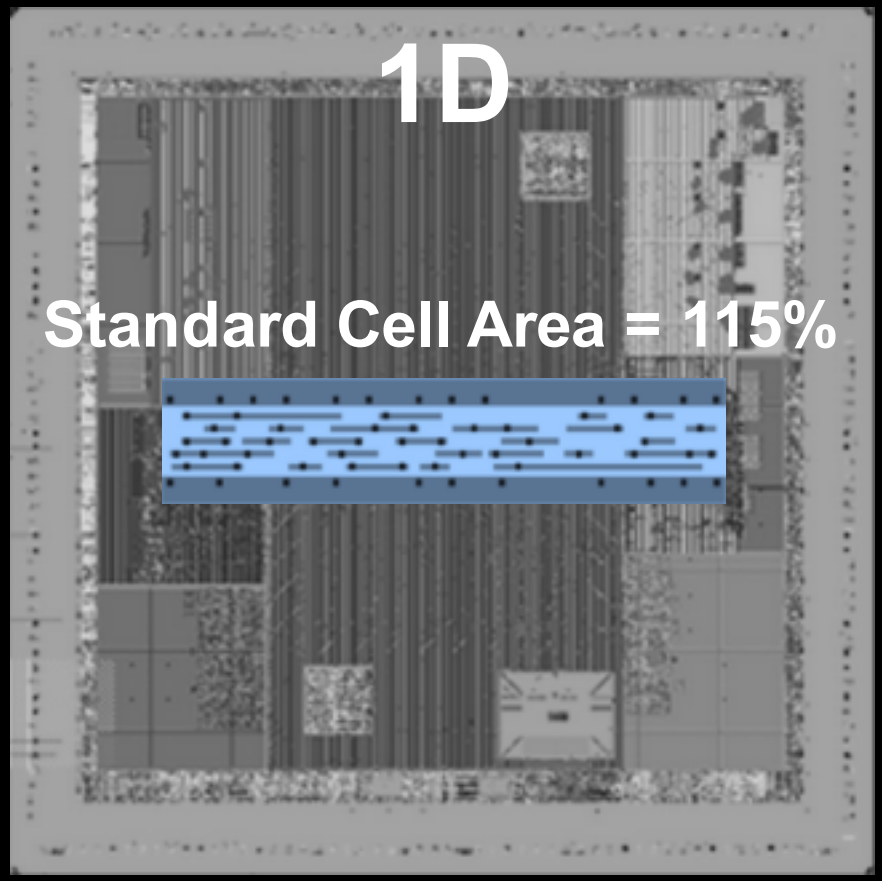
Design Implementation At ≤ 10 Nanometers

From 2D To 1D Routing AND Standard Cells



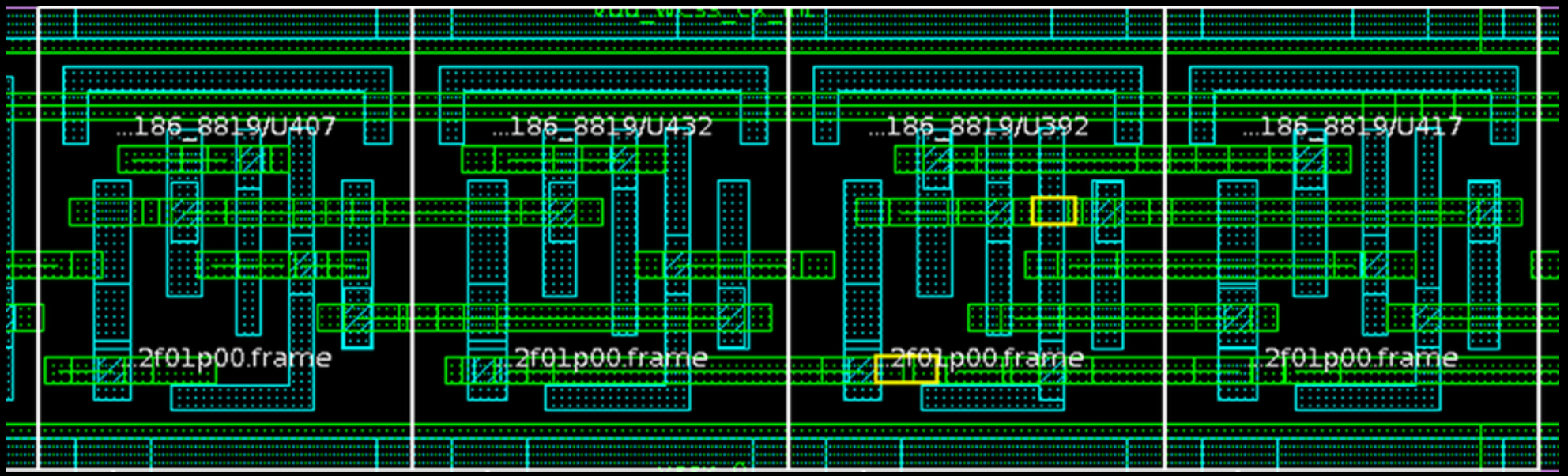


Source: M. van den Brink, ASML Investor Day 2014; Synopsys Research, 2017

Design Implementation At 7 Nanometers (70 Ångstroms)

End-of-Line Rules Violations at High Pin Count Cell Consecutive Placement Areas

When Pins Are Near Cell Boundary, Wire End Extend Beyond Boundary



Source: Synopsys Research, 2016

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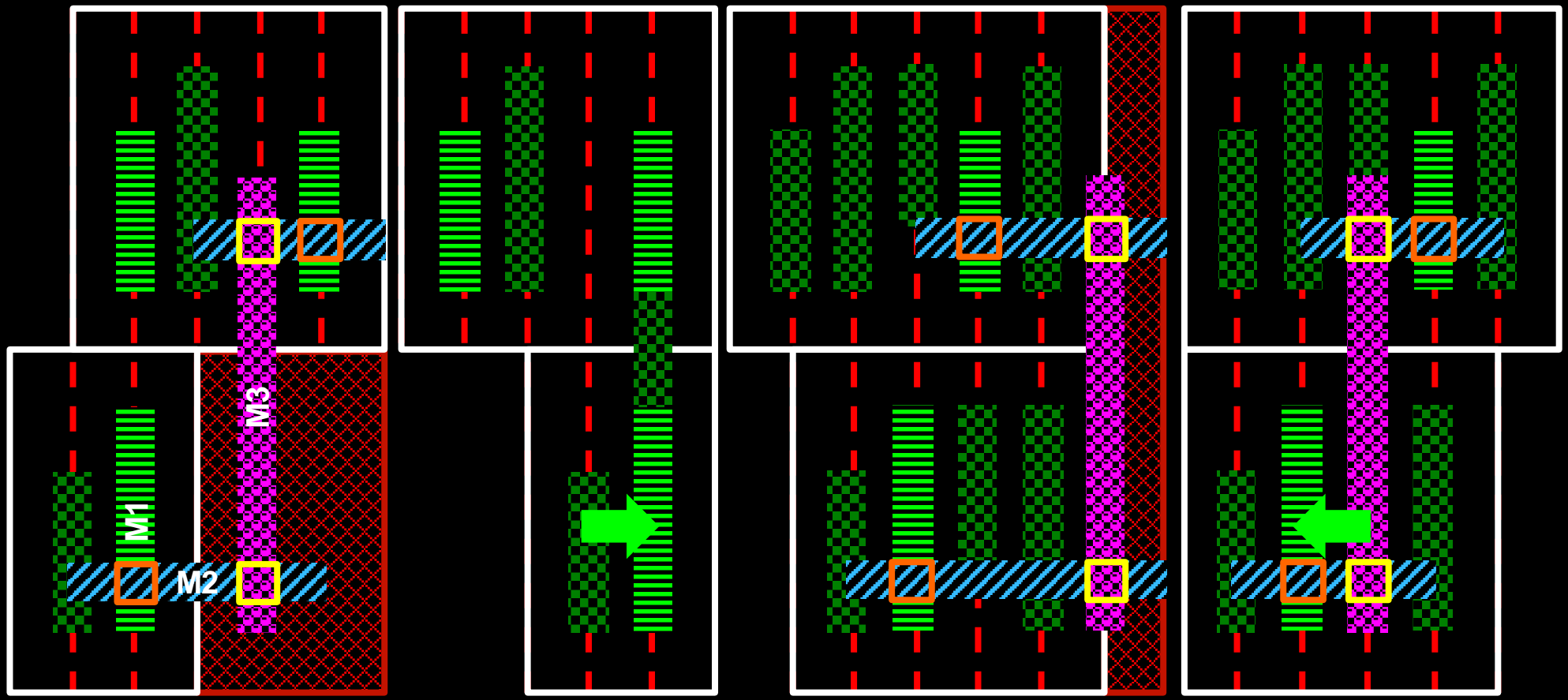
Design Implementation At 7 Nanometers

Placement Must Align Near-by Connected Pins Vertically to Allow Direct Connection on M1, and Avoid Connected Pins in Neighboring Rows Being One Track Off



Source: Synopsys Research, 2017

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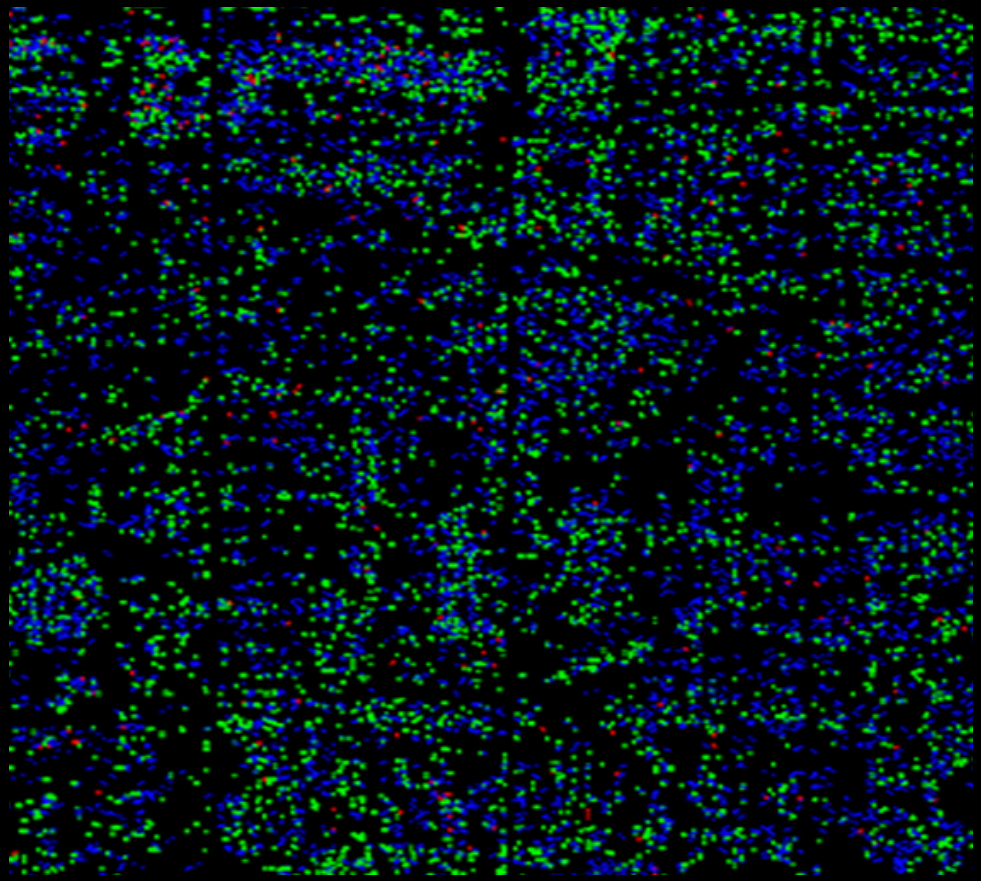
Design Implementation At 7 Nanometers

Vertical Pin Alignment-Aware Placement Reduces Routing Congestion



Source: Synopsys Research, 2017

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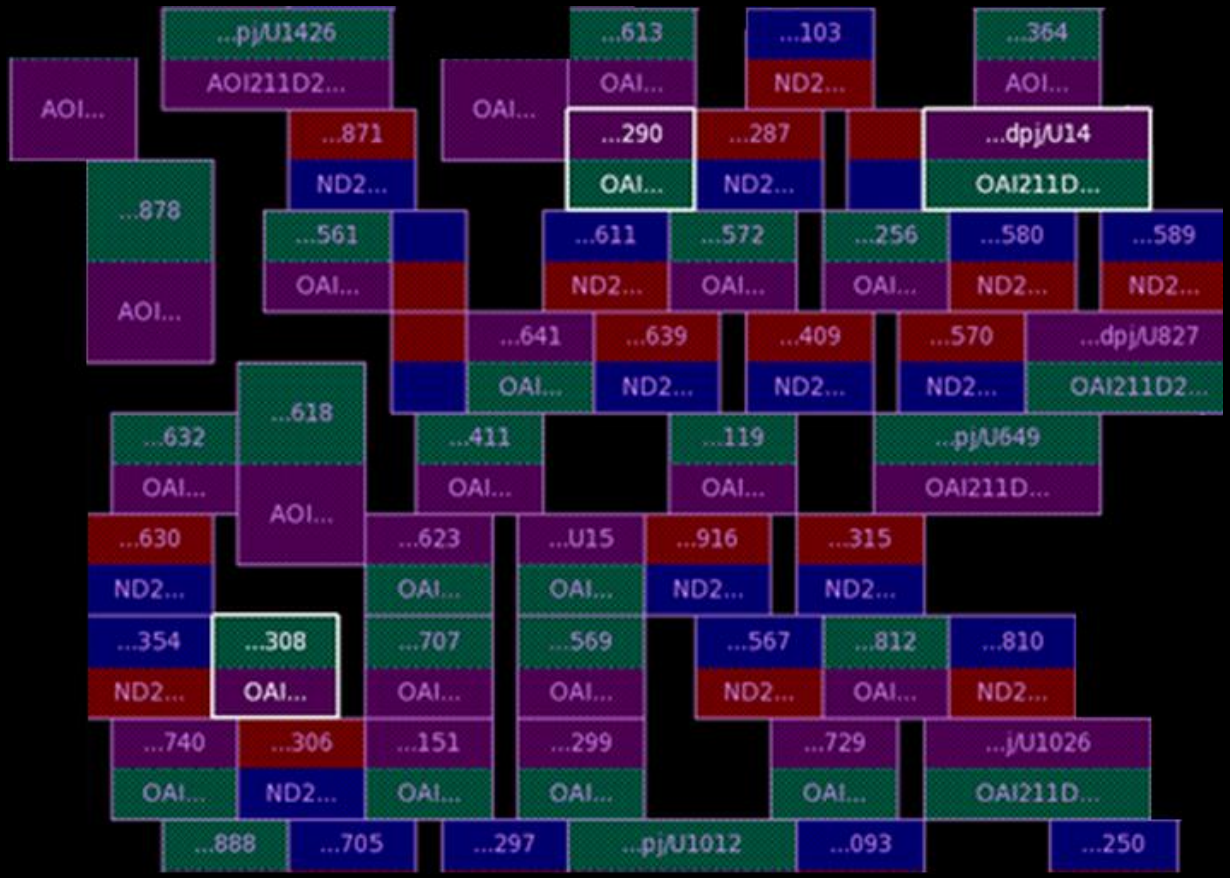
Design Implementation At 7 Nanometers

Placement Becomes Increasingly Restricted

More and More White Space Is Required to Achieve Legality



Source: Synopsys Research, 2017

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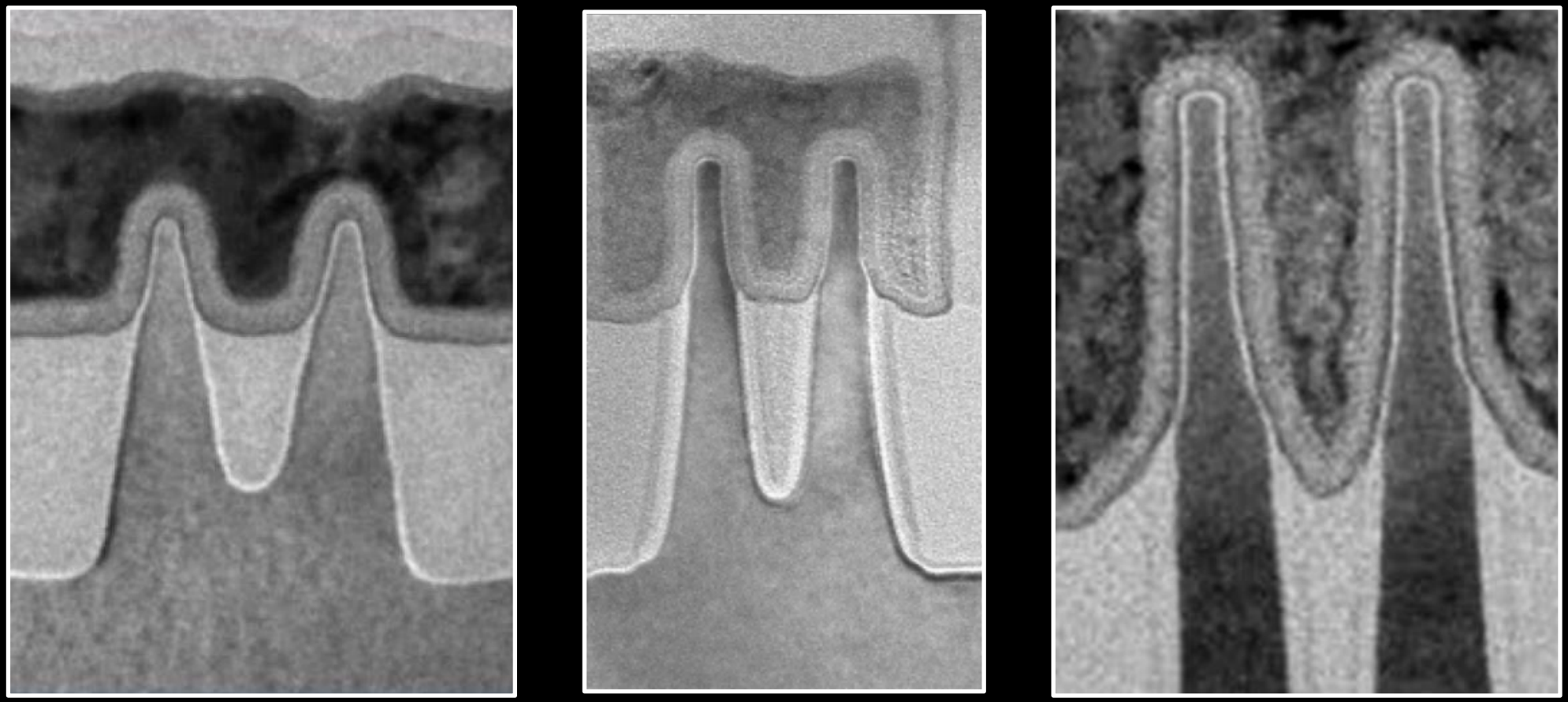
Device Implications – FinFET Prolonged Life Span

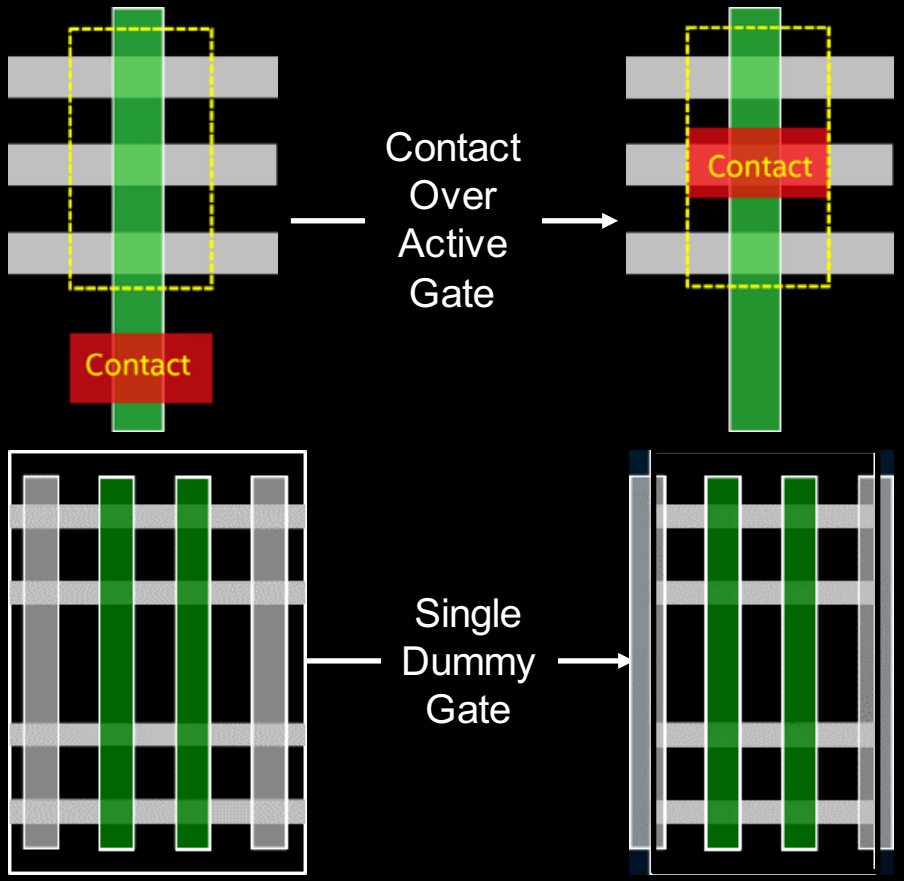
Taller/Closer Fins (Height/Pitch) : 34/60 ⇨ 42/42 ⇨ 53/34

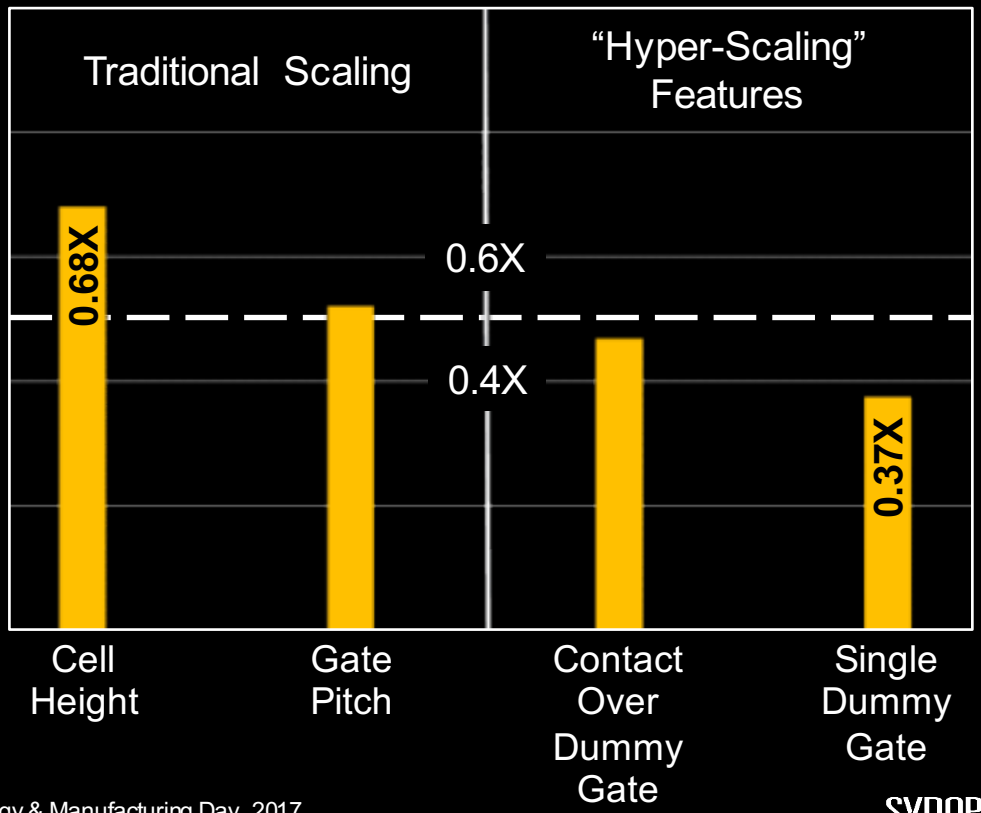


22, 14 & 10 Nanometer FinFET; Source: K. Mistry, Intel Technology & Manufacturing Day, 2017

Design Implementation At ≤ 10 Nanometers

Moore's Law Is Fueled by Single Bullet Weapons





Source: M. Bohr, Intel Technology & Manufacturing Day, 2017

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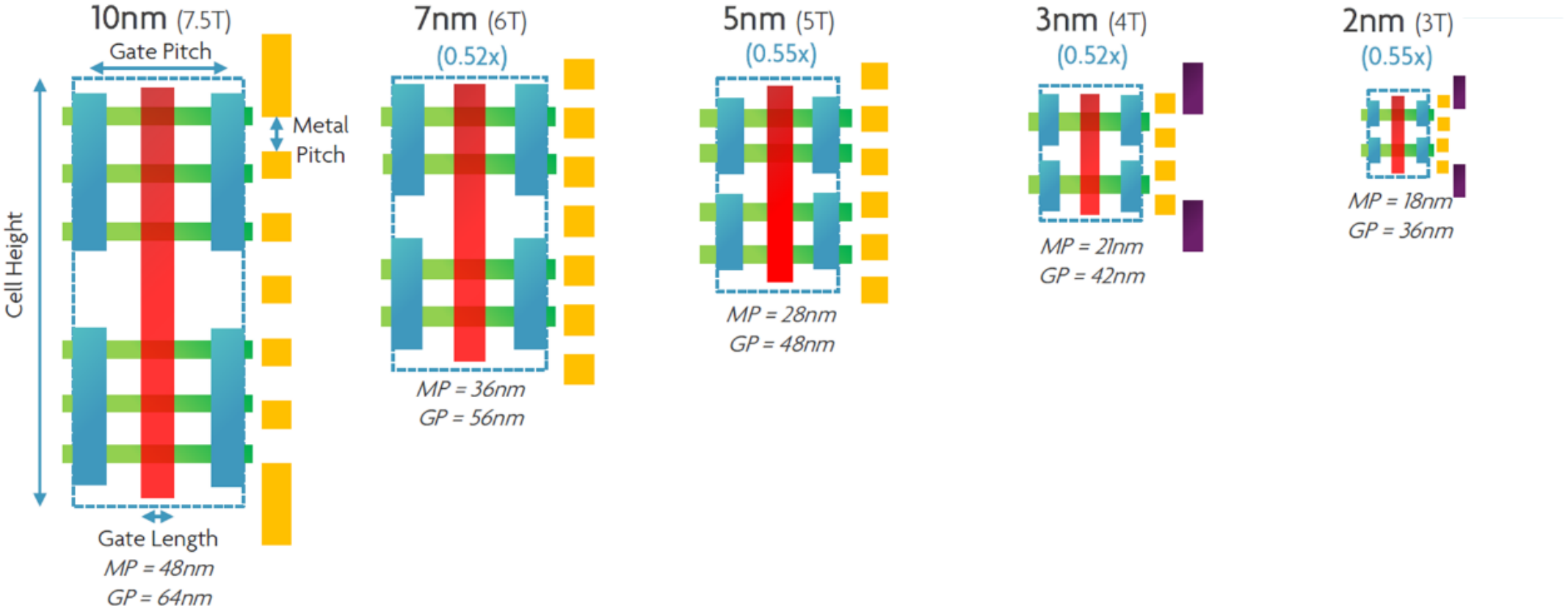
Design Implementation At ≤ 10 Nanometers

Caveat: Standard Cells Shrink, # of Pins Remains the Same



Source: IMEC Technology Forum, 2017

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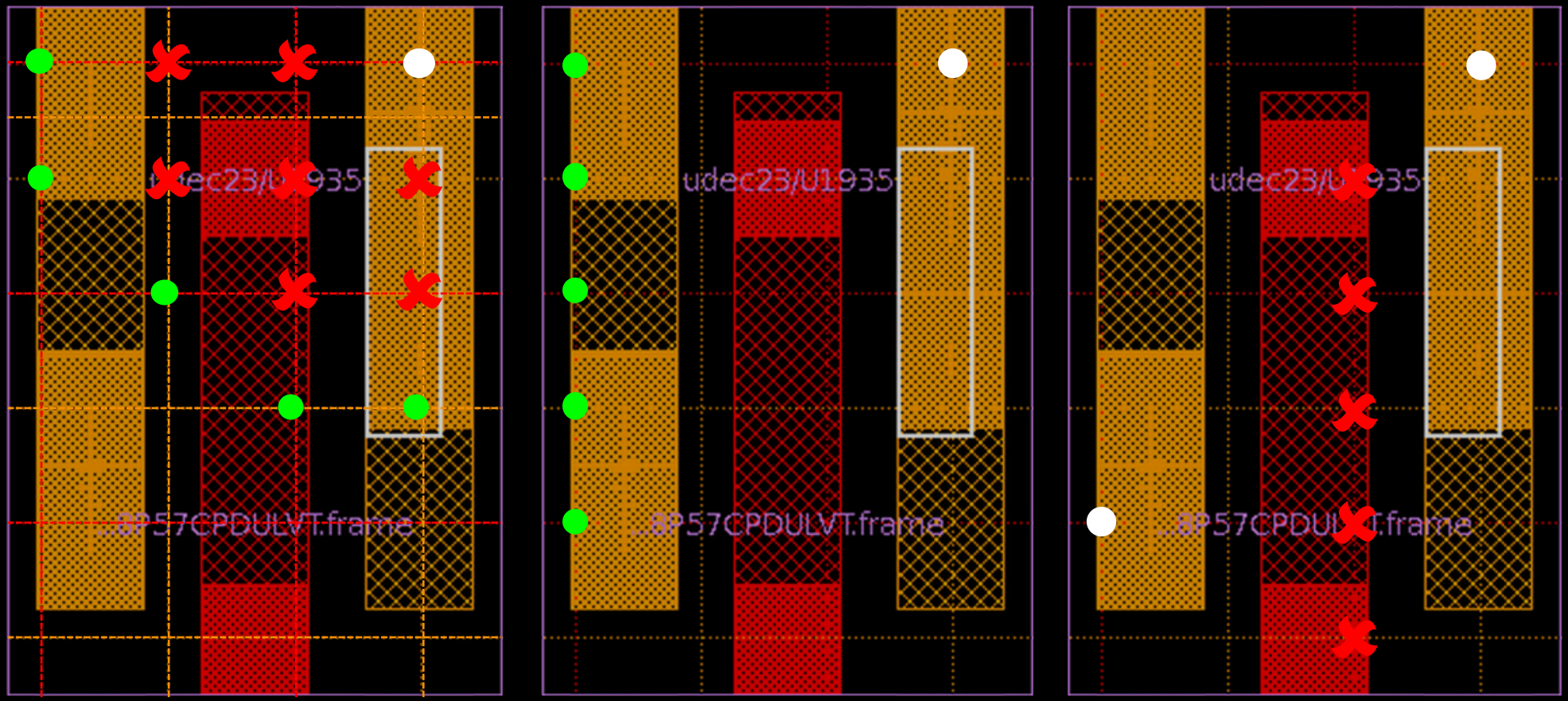
Design Implementation At 7 Nanometers

A Nanometer… Tic-Tac-Toe: a 4x6 Grid, P&R Must Route 3 Pins, But… There Are Only 4 Simultaneous Legal Access Points (Via Spacing Rule ≥ $2\sqrt{2}$ Grids)



Source: Synopsys Research, 2016

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Design Implementation At 7 Nanometers

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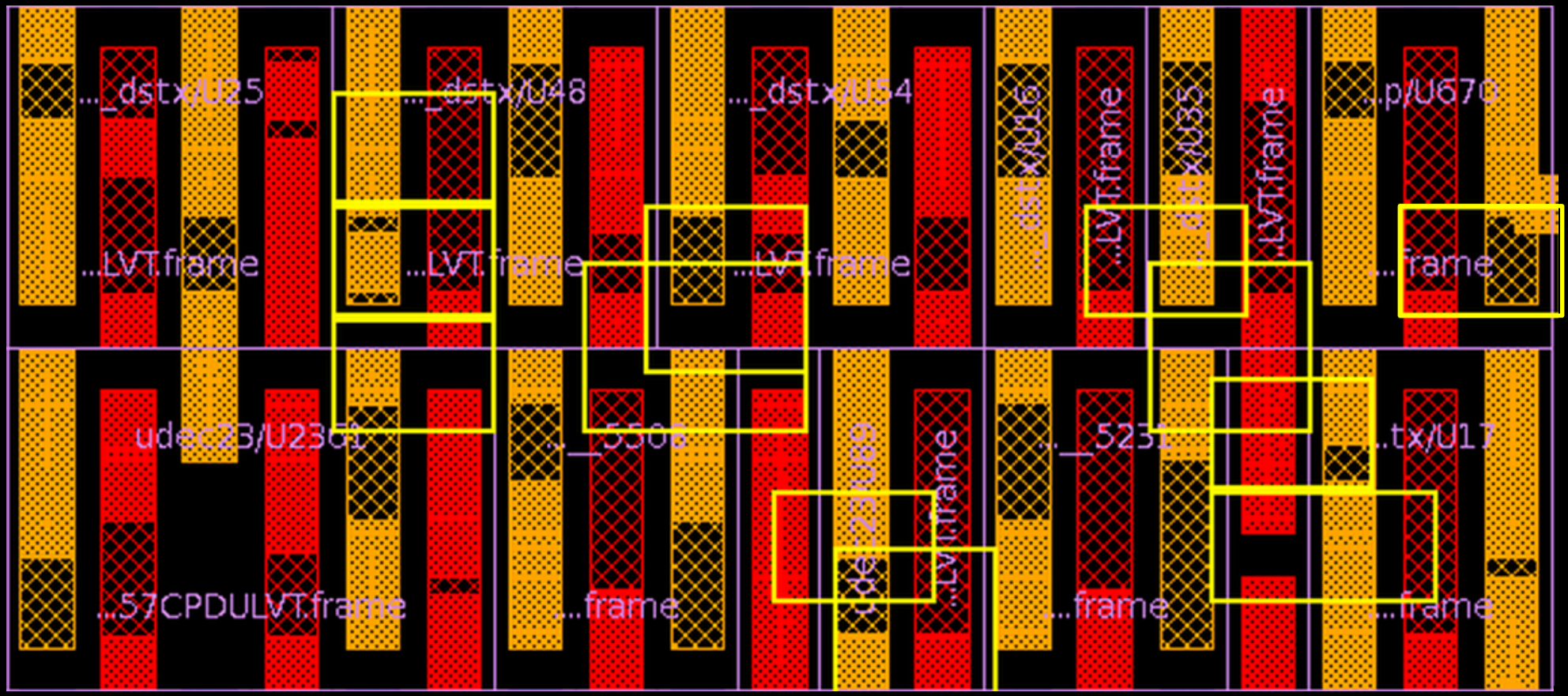

Source: Synopsys Research, 2016

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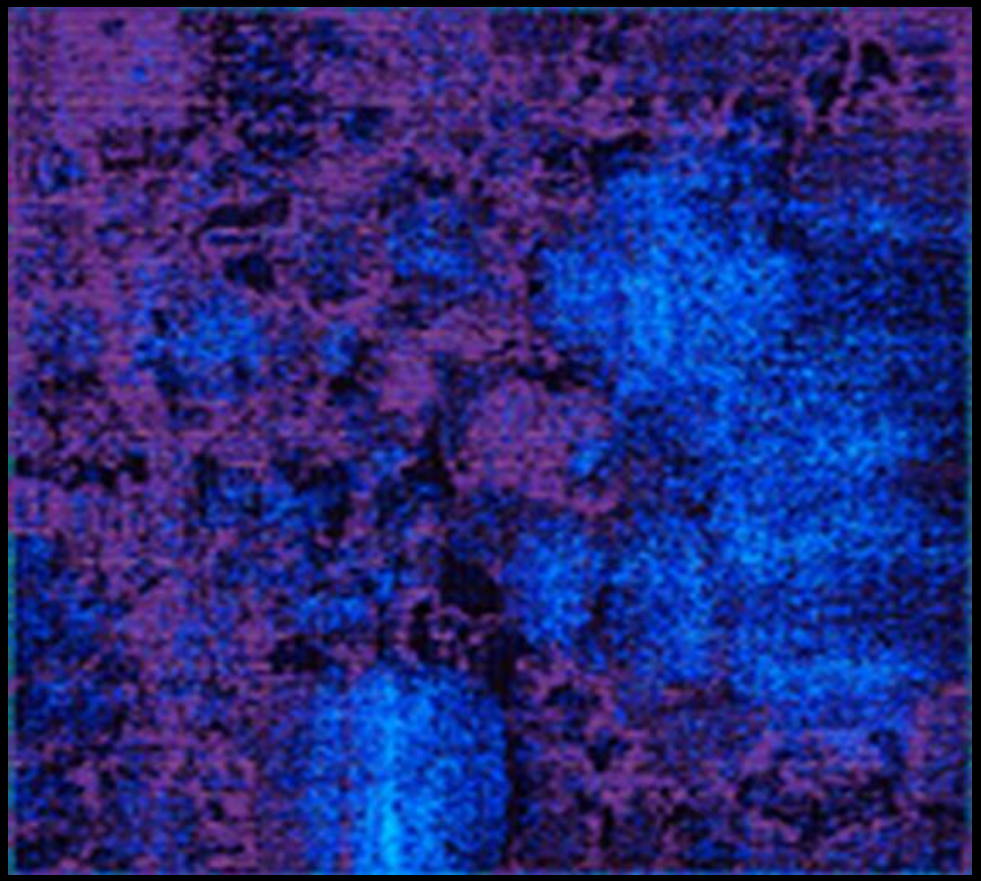
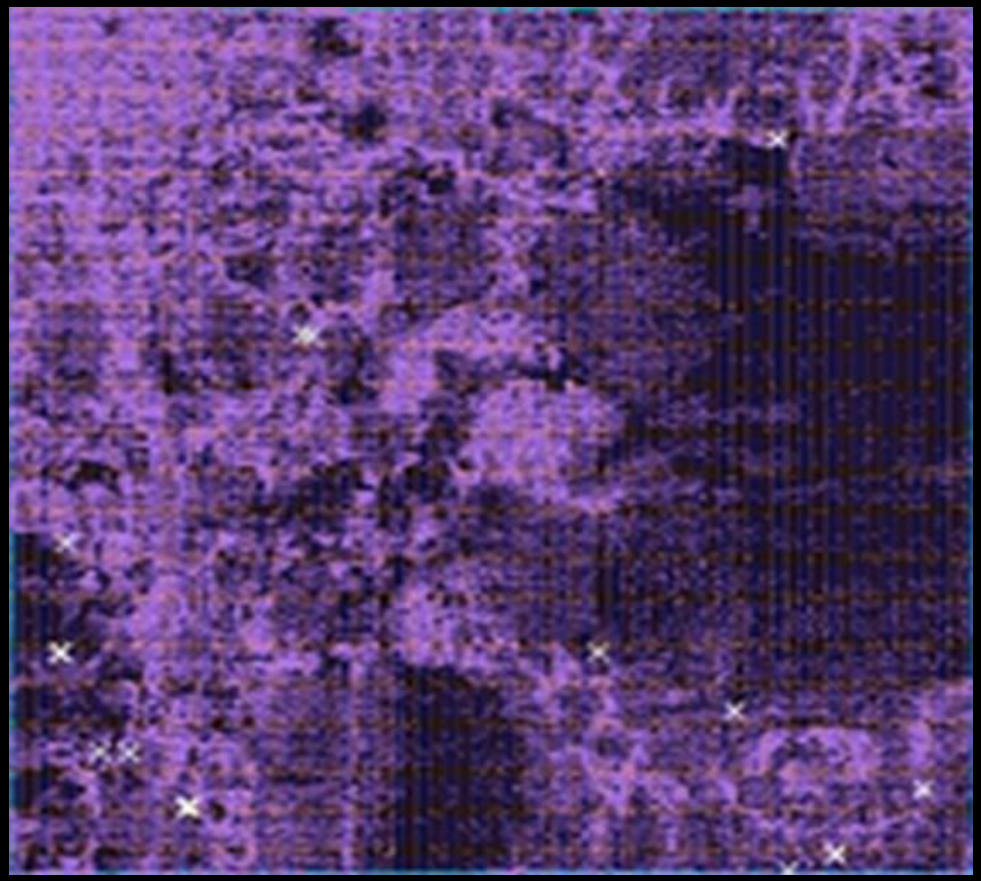
Design Implementation At 7 Nanometers

Pins Density & Accessibility-Aware Placement

Addresses/Mitigates Pins Density/Accessibility, and Routing Congestion Issues





Source: Synopsys Research, 2016

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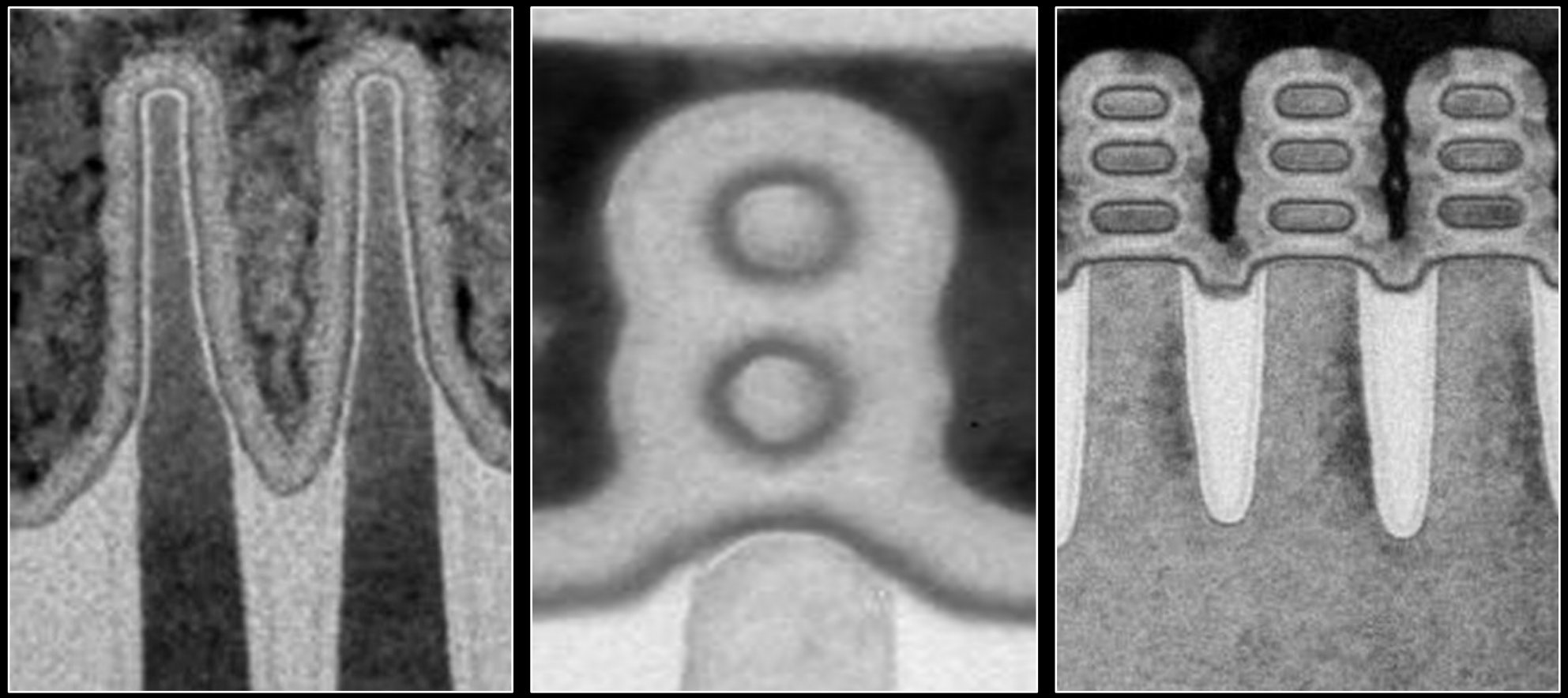
Device Implications – Beyond FinFET (At 3 Nanometers)

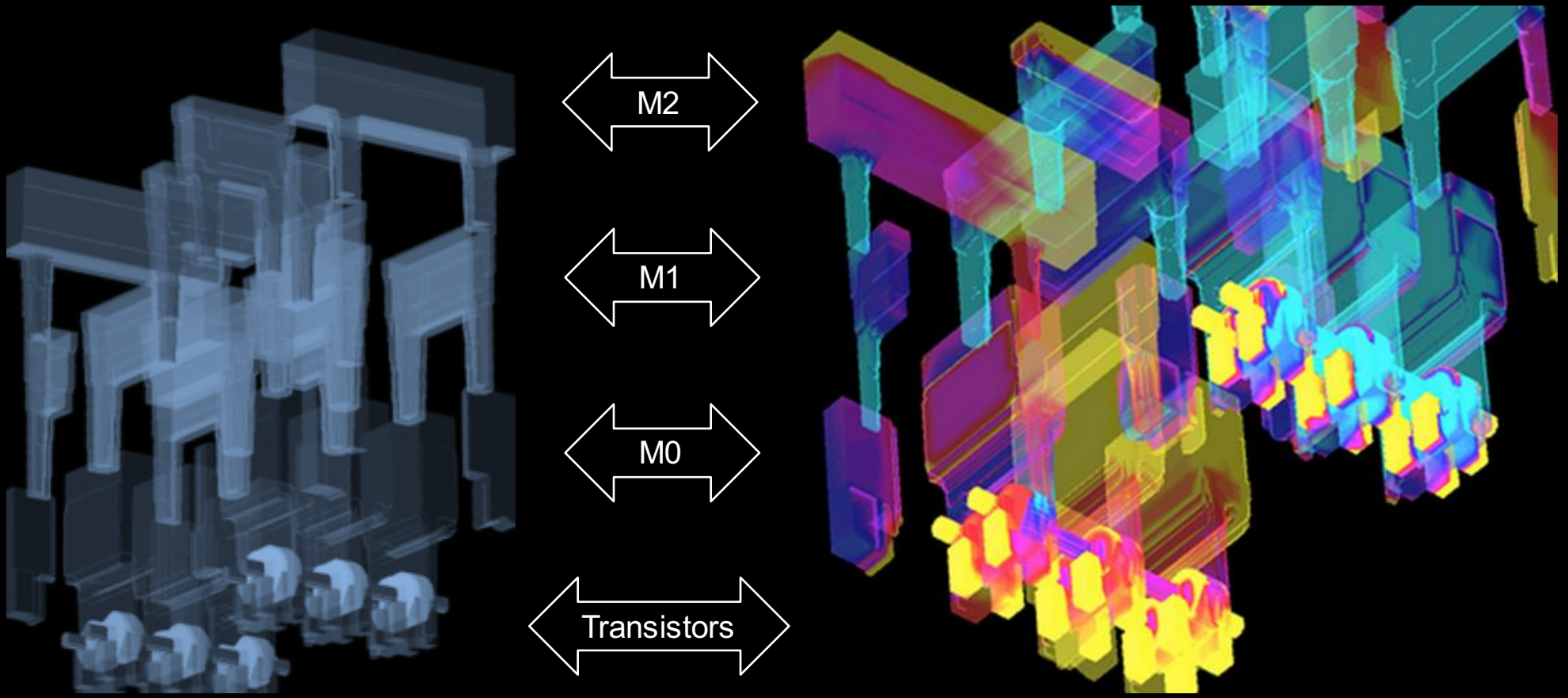
[Stacked] Nano-Wires, and Nano-Sheets



Source: K. Mistry, Intel Technology & Manufacturing Day, 2017; IMEC Technology Forum, 2017; IBM, 2017

Process Exploration At 5 Nanometers (50 Ångstroms)

2-Input NAND 3D Structure, and Current Flows



Source: V. Moroz, Synopsys, ISPD 2016

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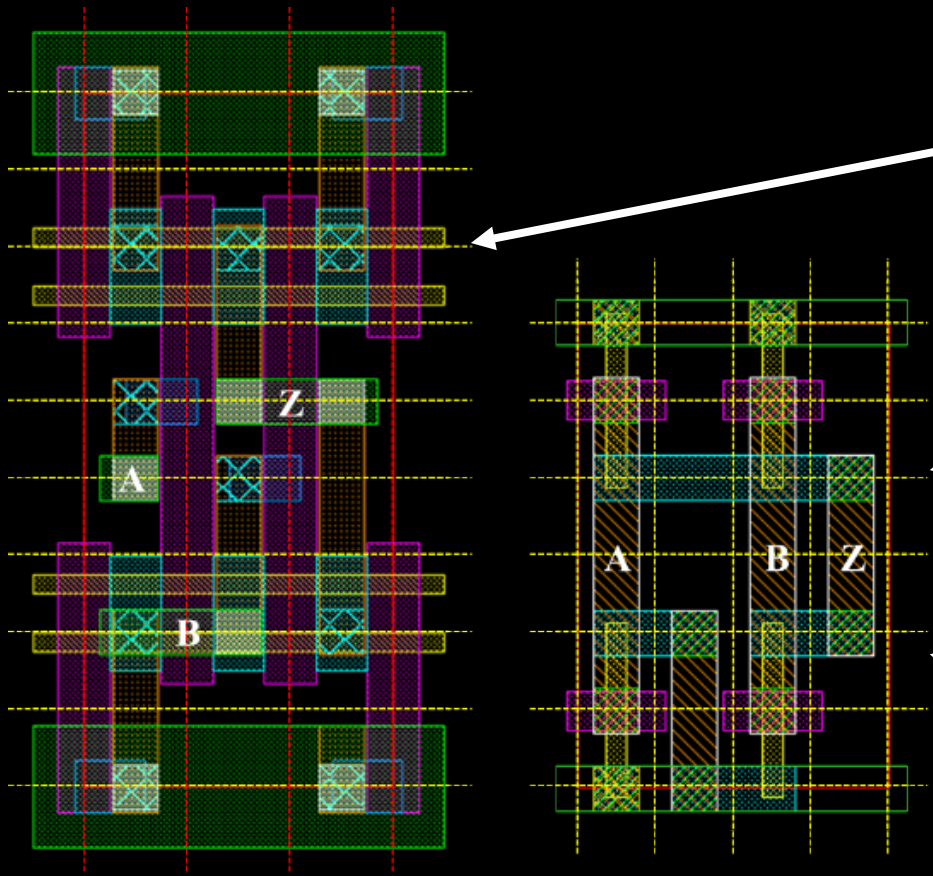
IP Exploration At 5 Nanometers

What If We Rotate The Fins ? 9-Track vs. 6-Track 2-Input NAND Layout

Gate Pitch = 48nm, M1 Pitch = 24nm, Fins Pitch = 48nm



6 routing tracks available
H grid ≠ V grid

5 routing tracks available
H grid = V grid

Large M1 landing pins
M2 transparent
(8% Lower Power)

Source: V. Moroz, Synopsys, ISPD 2016

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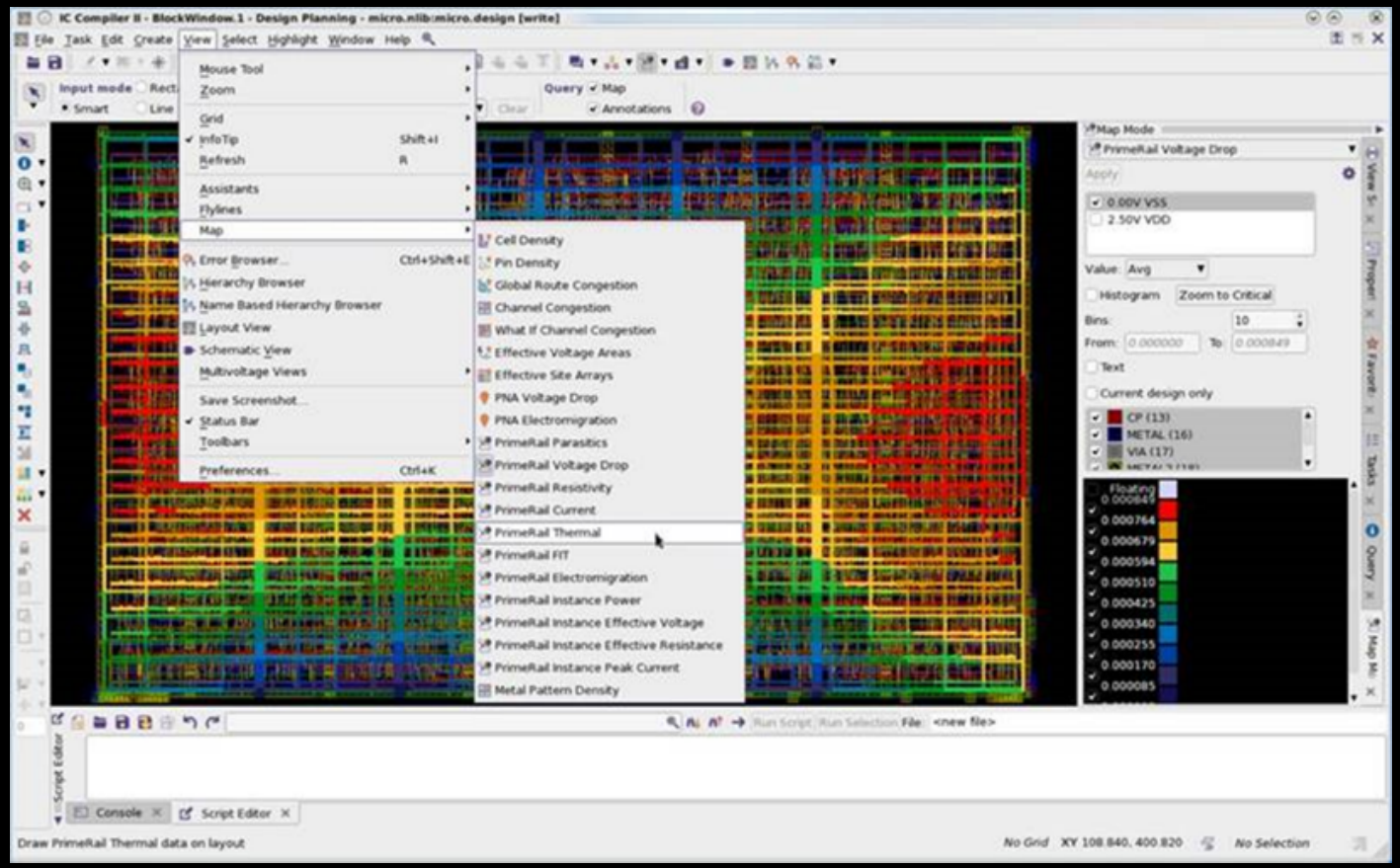
Temperature Distribution

How Do We Avoid "Hot Spots"? And how about New Structures?



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Agenda

Opening Remarks

⇨ **Where Do We Stand ? What Lies Ahead ?**

EUV Lithography & Non-Planar Devices

⇨ **Heterogeneous nD Integration**

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Opening Remarks

⇨ **Where Do We Stand ? What Lies Ahead ?**

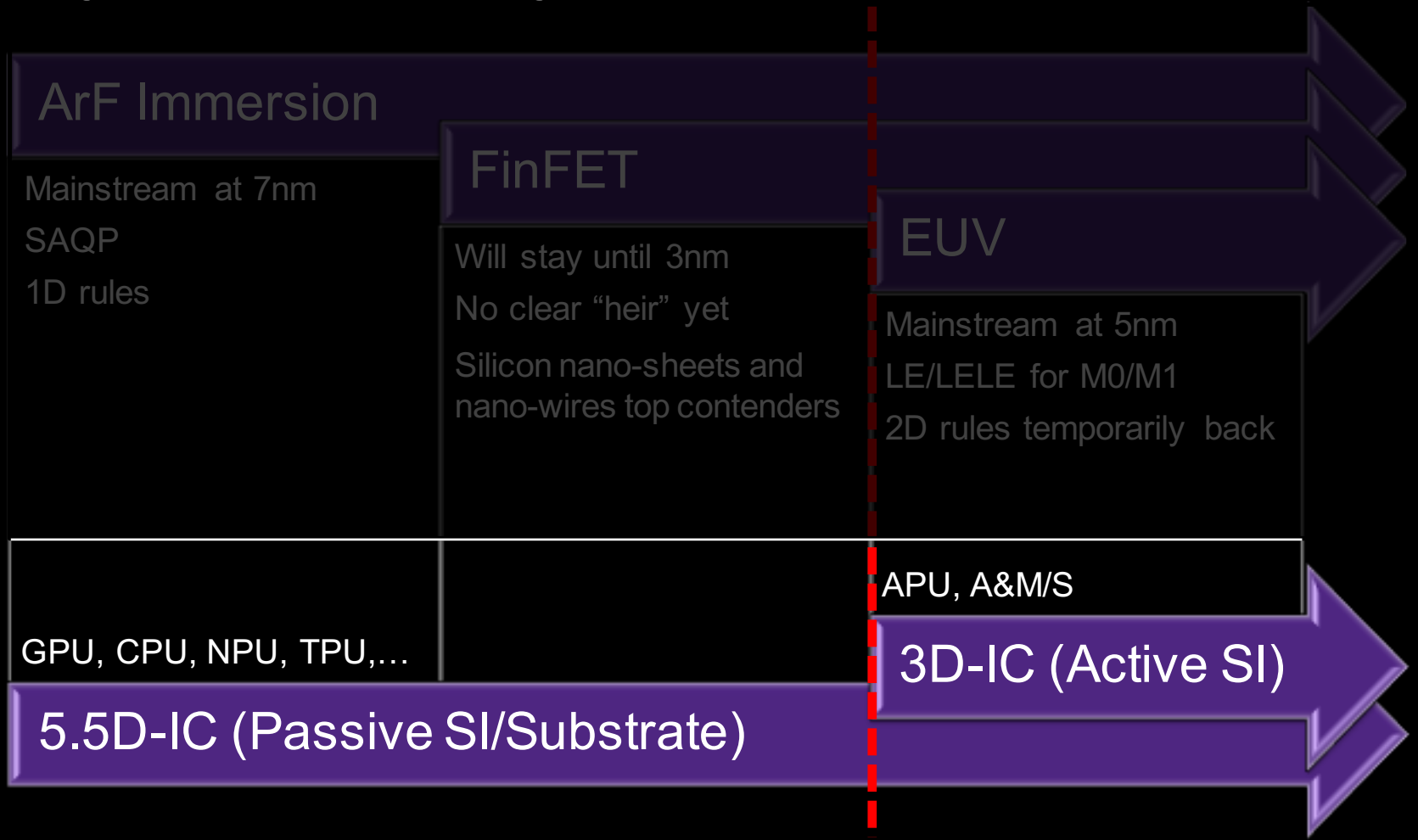
EUV Lithography & Non-Planar Devices

⇨ **Heterogeneous nD Integration**

Kazimir Malevich, Two Dimensional Self-Portraits, 1915

Where Do We Stand ? What Lies Ahead ?

Heterogeneous nD Integration



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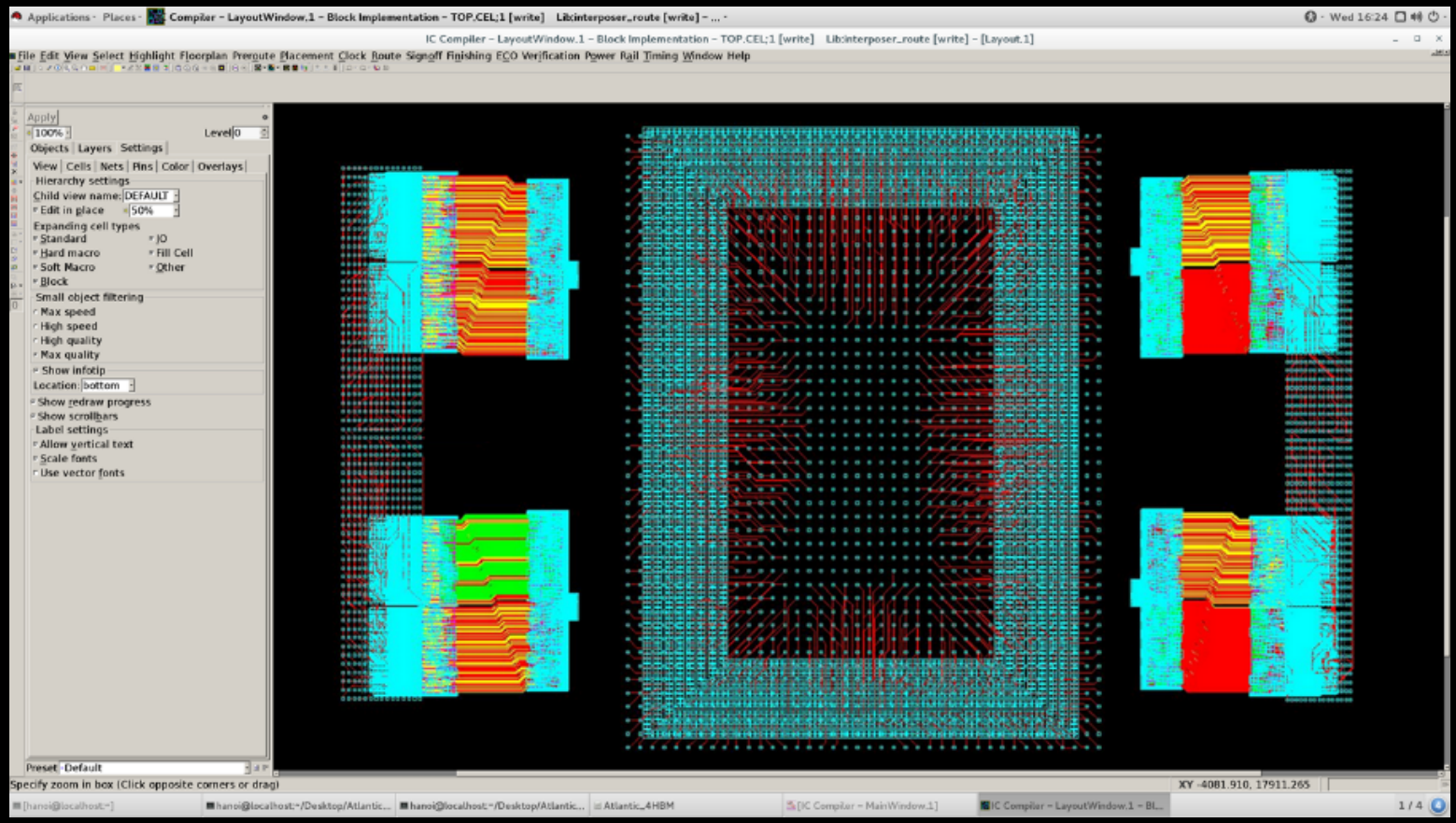
Integration Implications – Beyond The Die

Multiple Die/Stacks Onto Multiple Silicon Interposers



Source: Synopsys Research, 2017

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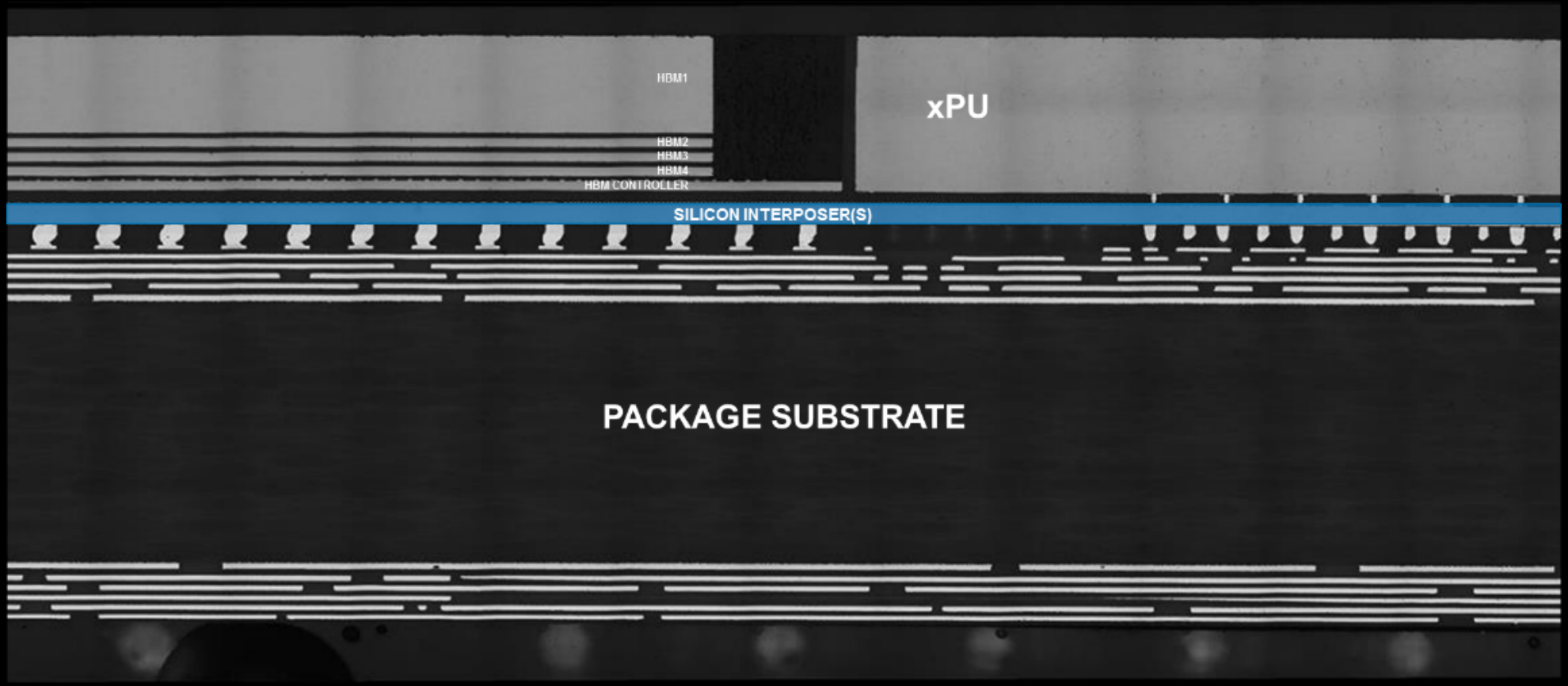
Integration Implications – 5.5D-IC

Multiple Die/Stacks Onto Multiple Silicon Interposers



"Pascal" 5.5D-IC (3D + 2.5D) Integration; Source: L. Nyland, et al., NVIDIA, GPU Technology Conference 2016

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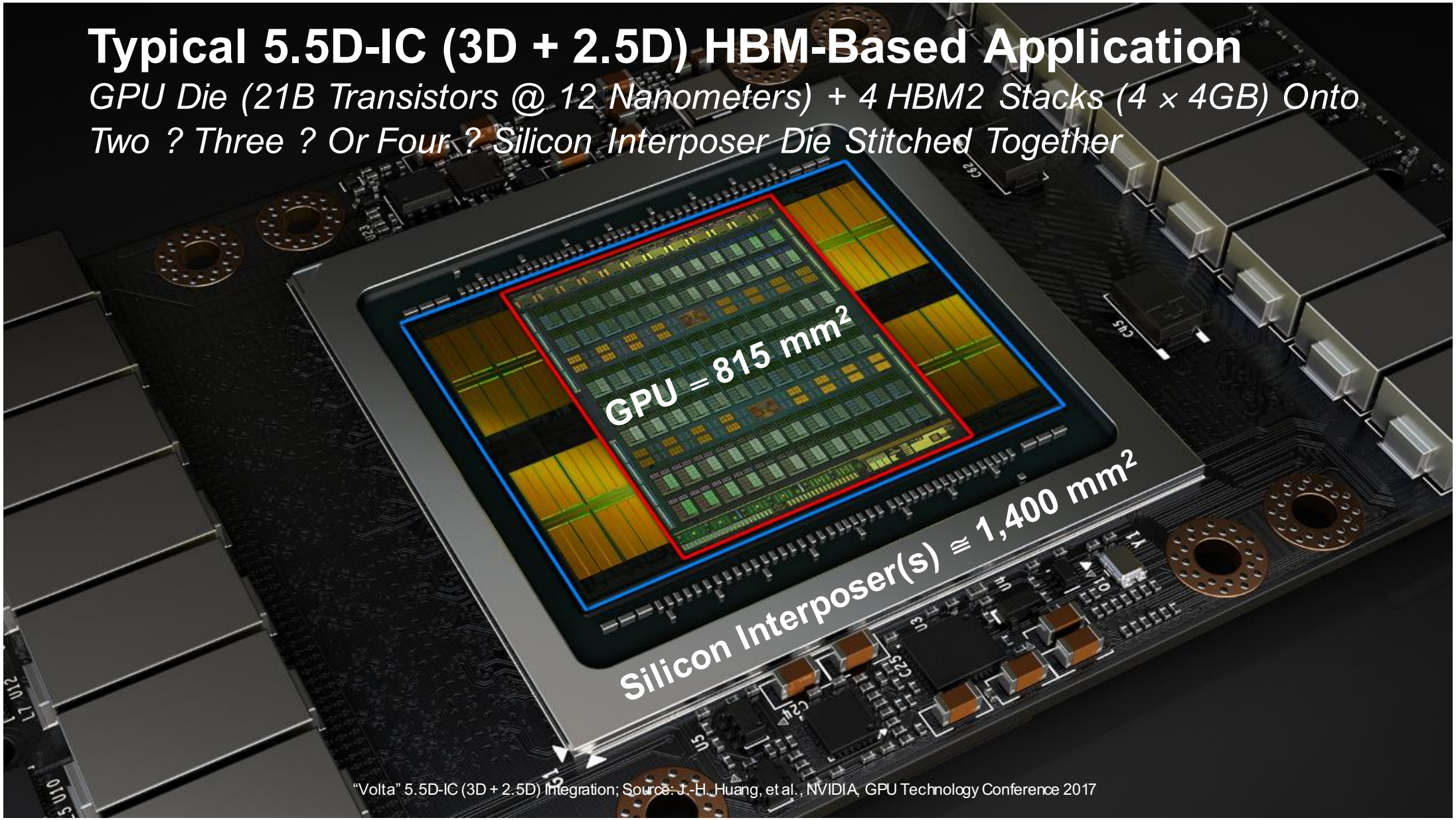
Typical 5.5D-IC (3D + 2.5D) HBM-Based Application

GPU Die (21B Transistors @ 12 Nanometers) + 4 HBM2 Stacks (4 × 4GB) Onto Two ? Three ? Or Four ? Silicon Interposer Die Stitched Together



"Volta" 5.5D-IC (3D + 2.5D) Integration; Source: J.-H. Huang, et al., NVIDIA, GPU Technology Conference 2017

Integration Implications – 3D vs. Monolithic 3D

Coarse vs. Fine Grain, Die vs. Transistors

We are at the dawn of 3D-IC integration

Only “discrete” 3D is ready for the primetime

Its impact on synthesis is very limited (partitioning)

However, monolithic 3D may be around the corner

Increasingly complex logic functions/IP could be vertically implemented, in different variants

The impact on synthesis may be profound

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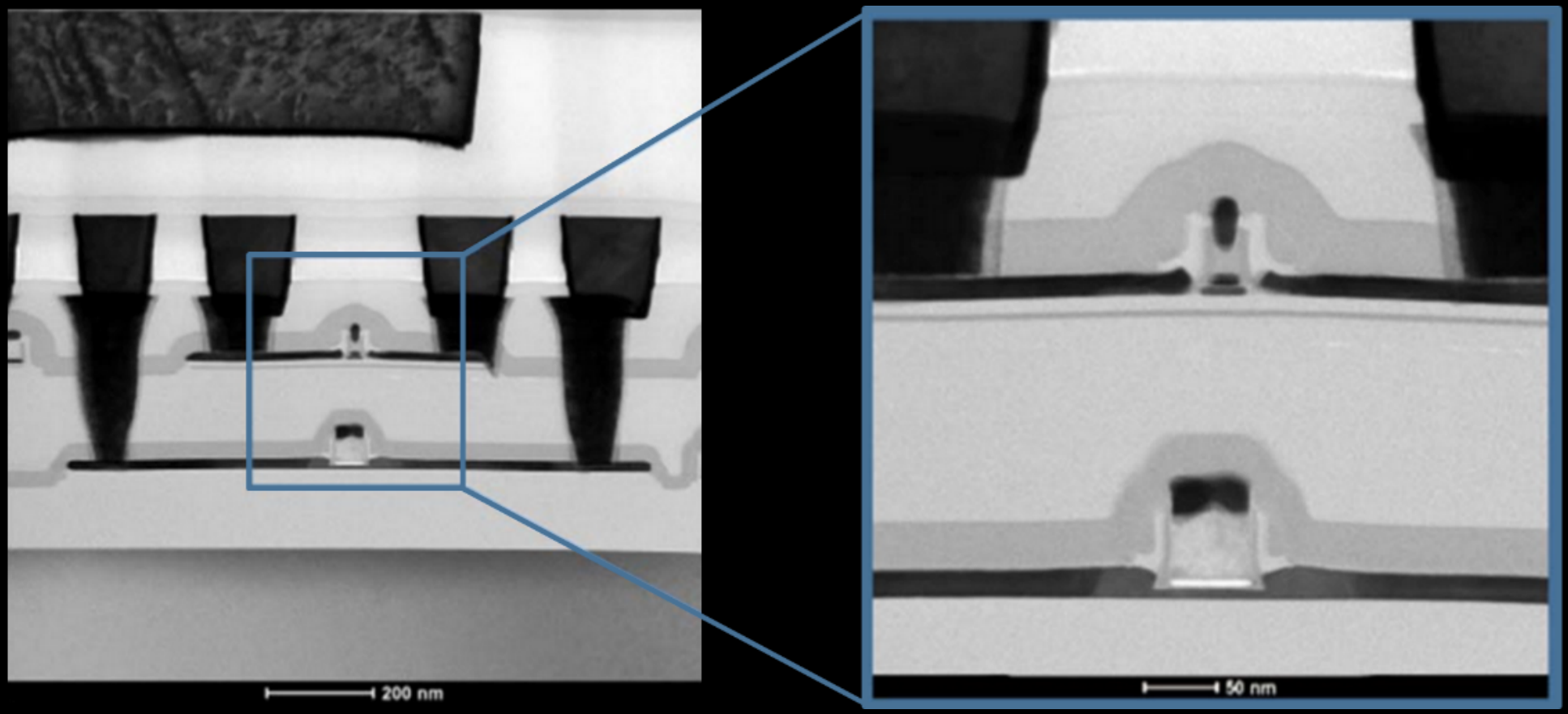
Integration Implications – Monolithic 3D

Multiple Tiers Stacked One on Top of Another



Source: P. Batude, et al., LETI, VLSI 2011

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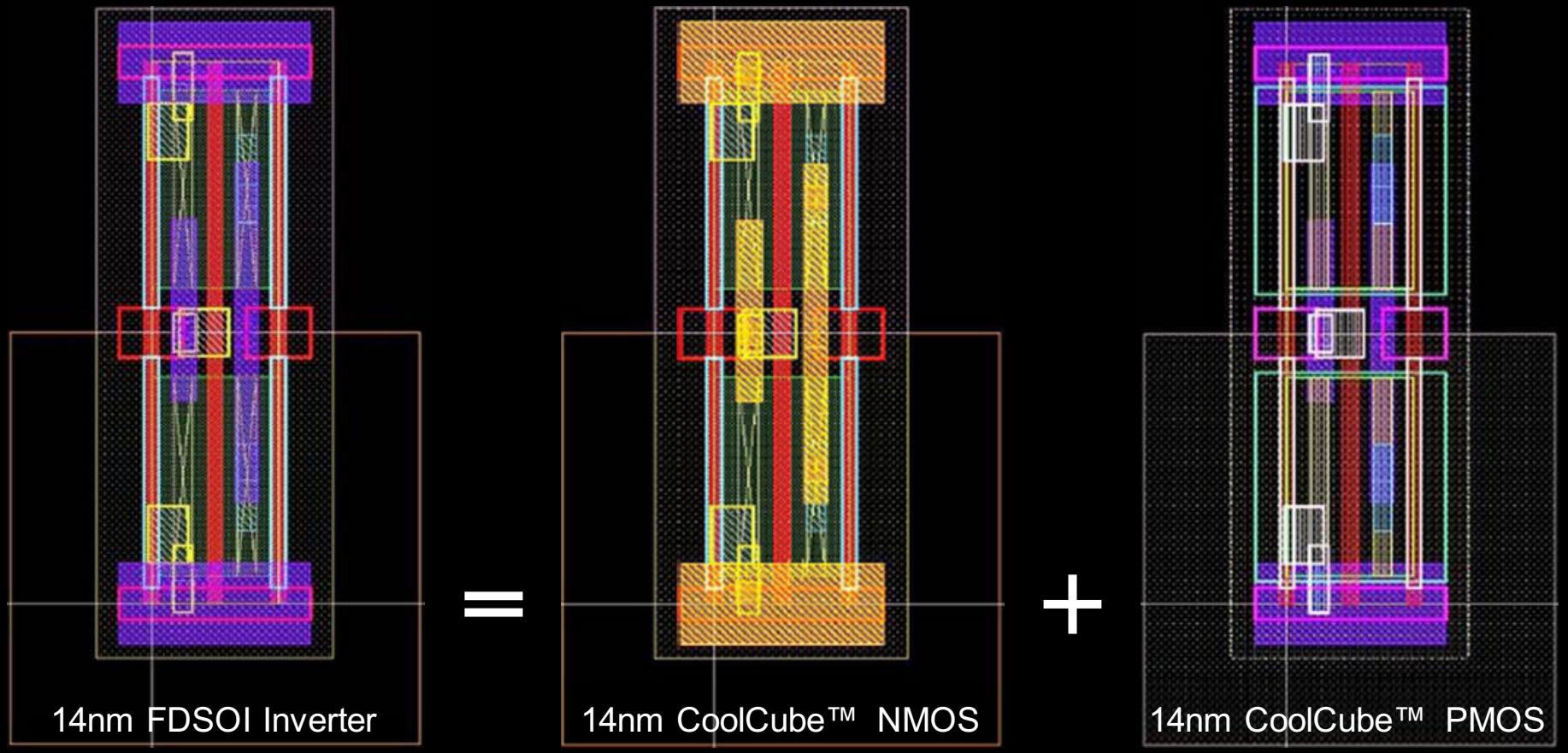
Some Implications On Logic Synthesis : Monolithic 3D

Placement Trivial for Simple Gates, May Get Awfully Complex



Source: G. Cibrario, et al., LETI, 3DIC 2016

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Agenda

Opening Remarks

Where Do We Stand ? What Lies Ahead ?

- EUV Lithography & Non-Planar Devices
- Heterogeneous nD Integration

⇨ **Closing Remarks**

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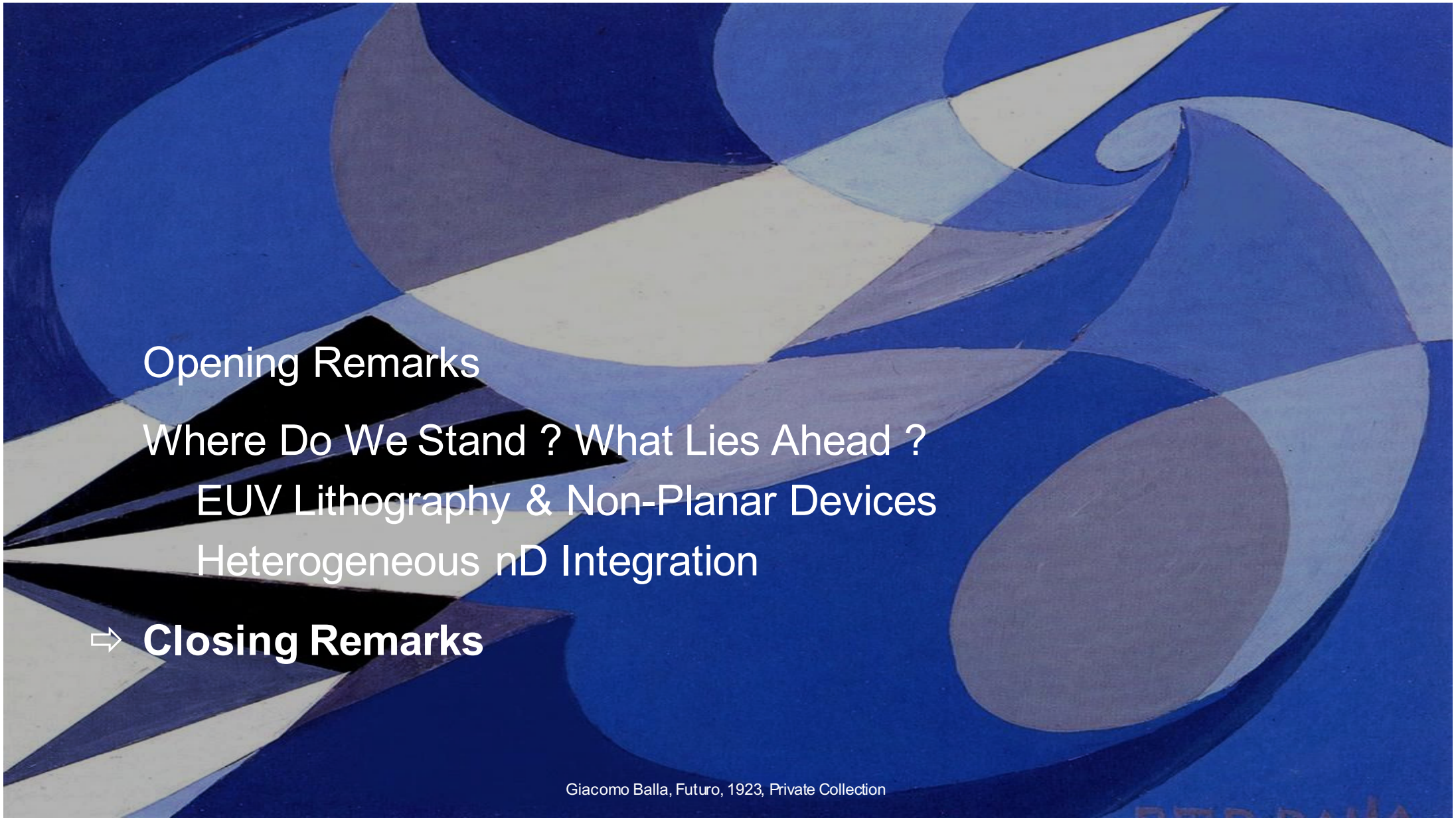


Opening Remarks

Where Do We Stand ? What Lies Ahead ?

EUV Lithography & Non-Planar Devices

Heterogeneous nD Integration

⇨ **Closing Remarks**

Giacomo Balla, Futuro, 1923, Private Collection

Closing Remarks

A lot of the “implications” of the coming semiconductor technologies have a profound impact on synthesis

Sheer complexity remains the #1 challenge

1T transistors at 3nm (30Å) translate into up to 100B placeable instances

The # of polygons & (L)RC values may exceed

$1P = 10^{15} = 50$ bits

Closing Remarks

Transistors shrink much faster (30% linear, 50% area)
than interconnect (20%)
The # of pins/gate remains the same,
accessibility/routability is the key problem
Synthesis is mostly physical (as opposed to logic)
3D integration will bring challenges beyond the die

Closing Remarks

At about 2 nanometers CMOS lifespan may, finally, come to an end

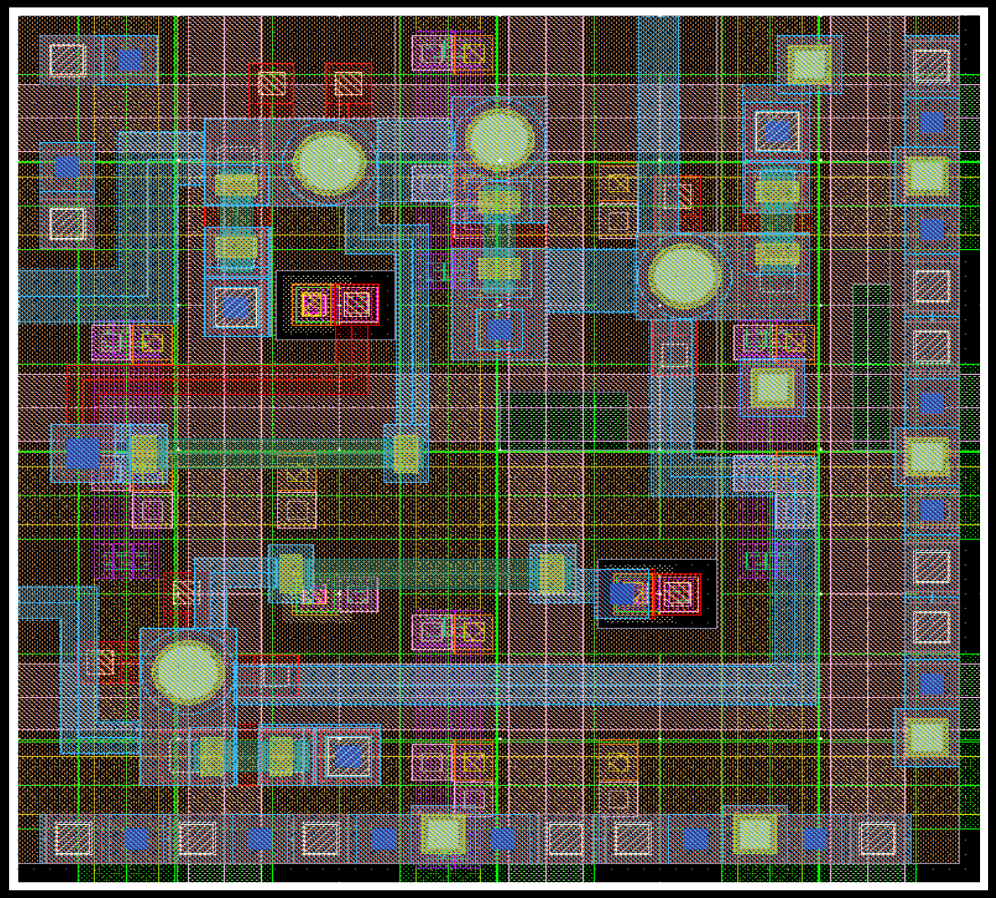
The quest for a general purpose replacement is still on-going

Super-conducting electronics is an emerging candidate, and may be a solid foundation for quantum computing

It poses significant challenges to synthesis

Some Implications On Logic Synthesis : JJ-Based SCE

Super-Conducting Electronics & Quantum Computing



4 °K Required

Reversible logic only

10,000X larger than CMOS

1,000X faster than CMOS

1,000X lower power

ZERO interconnect R

ERSFQ D Flip-Flop, Designed for the MIT Lincoln Laboratories SFQ5ee Process; Source: Hypres, 2017


The BUCK STOPS here!

Some Implications On Logic Synthesis From The Coming Semiconductor Technologies

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Synopsys, Inc.